RCA

MASTER

CTC 175/176/177

TECHNICAL TRAINING MANUAL

FOREWORD

This publication is intended to aid the electronic technician in servicing the CTC175/176/177 television chassis. It will explain the theory of operation, highlighting new and different circuits associated with the digitally controlled chassis. This manual focuses on: PIP, Tuner-On-Board and System Control circuitry. It is designed to help the technician become more familiar with the chassis layout, increase confidence and improve overall efficiency in servicing the product.

Note: This publication is intended to be used only as a training aid. It is not intended to replace service data. Thomson Consumer Electronics Service Data for these instruments contains specific information about parts, safety and alignment procedures and must be consulted before performing any service. The information in this publication is as accurate as possible at the time of publication. Circuit designs and drawings are subject to change without notice.

SAFETY INFORMATION CAUTION

Safety information is contained in the appropriate Thomson Consumer Electronics Service Data. All product safety requirements must be compiled with prior to returning the instrument to the consumer. Servicers who defeat safety features or fail to perform safety checks may be liable for any resulting damages and may expose themselves and others to possible injury.

All integrated circuits, all surface mounted devices, and many other semiconductors are electrostatically sensitive and therefore require special handling techniques.

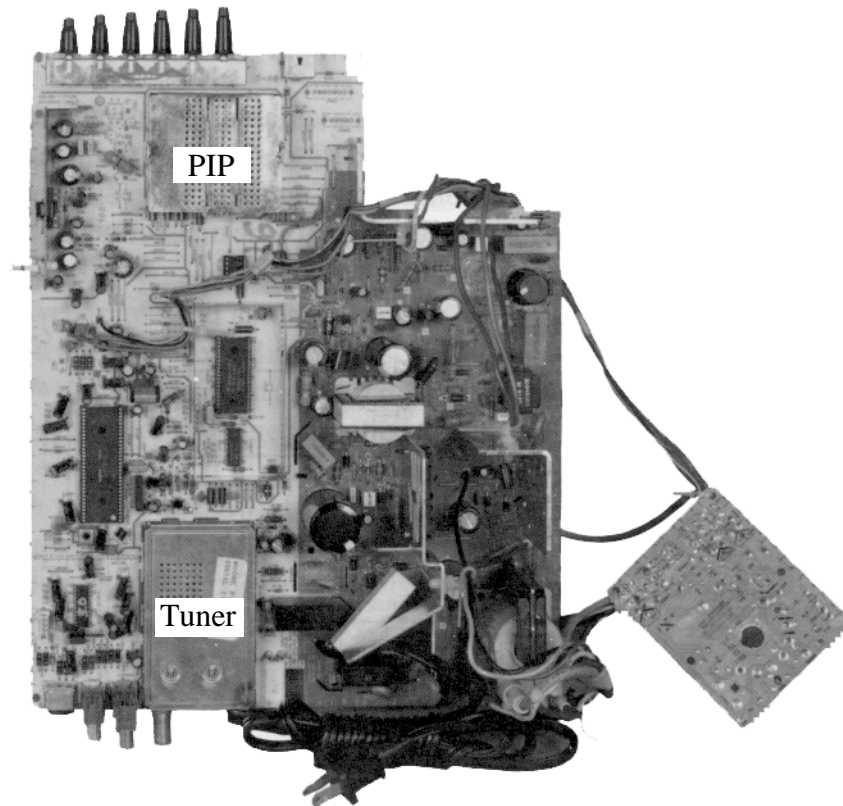# Table of Contents

Figure 1, F25190

Figure 2, CTC177 Chassis

The CTC175/176/177 chassis is a new concept in television design. All three chassis are very similar, with the primary differences being features and power supply. The CTC175 chassis is a hot chassis with a linear regulator. Consequently, this version does not have audio or video jacks on the back. The CTC176 and CTC177 have a switching regulator that allows for a cold chassis.

OVERVIEW

Four innovations are incorporated in these chassis. First, all the alignments are performed digitally using the remote control. There are no potentiometers on the chassis. All alignments are stored in the EEPROM. Second, the tuner is located on the main chassis circuit board. This requires the tuner to be serviced down to the component level where it used to be a replaceable assembly. Third, the fully featured models contain a new PIP (picture in picture) circuit. It too is located on the main board and is much more integrated than similar circuits in the CTC169 chassis. There are only two IC's: the PIP processor, U2901 and the SRAM memory, U2902. The increased integration makes troubleshooting much easier. Fourth, later versions of this chassis will contain built-in closed caption decoders for the hearing impaired. This circuitry is primarily contained within the system control microprocessor, U3101, and will require practically no service from the technician.

Different models support 20", 25", 27" and 31" screen sizes. Various option packages will accompany the different sets. Fully featured sets will have the new PIP circuit with S-Video *In* jacks with the standard Video/Audio *In/Out* jacks. The composite video jacks are used for the PIP source, as the S-Video is not routed through the PIP circuit. Stereo audio with HI-FI out jacks are also included as options.

Power Supply

The CTC176/177 power supply is a variable frequency/variable pulse width hybrid IC power supply. U4101, the hybrid IC, contains most of the components including the power switching FET (Field Effect Transistor). The switching device turns on and off inducing a voltage into the secondary of the transformer. The lower the frequency, the more energy is transferred to the secondary.
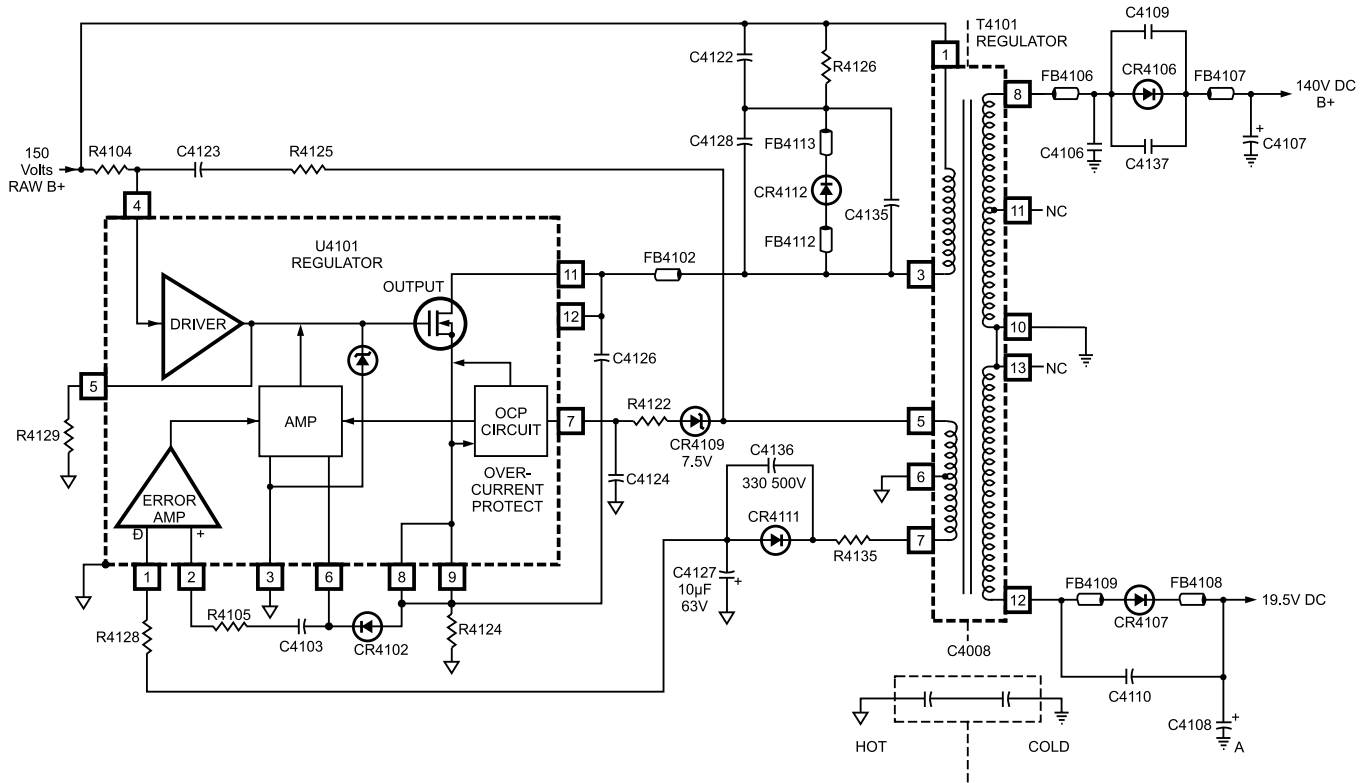
Figure 3, CTC176/177 Power Supply

When power is first applied to the set, approximately 150 VDC raw B+ is developed by the bridge rectifier (CR4001 - CR4004) and filter capacitor (C4007). This is applied through the primary winding of T4101 pins 1 and 3 to U4101 pins 11 and 12. Pins 11 and 12 are connected to the drain of the power FET inside U4101. The source of the power FET is connected to pins 8 and 9. These pins are connected to ground through R4124. The start-up resistor (R4104) provides enough bias to gate the FET on through pin 4 of the IC. When the FET is turned on, the drain current flows through the primary winding of T4101, through the FET to ground. Current flowing in the primary induces a voltage between pins 5 and 6 of the transformer. This voltage is coupled from pin 5 through R4125 and C4123 to pin 4 of the regulator IC. The polarity of the voltage at pin 4 is such that it turns the FET on harder. As more current flows through the FET, the greater the voltage drop across R4124, the FET source resistor. The voltage will eventually become

large enough to turn on the over-current protection circuit (OCP) inside U4101. This will cause the FET to turn off. When the FET turns off, energy transfers to the secondary windings of T4101 charging C4107 and C4108. This repeats for several cycles and stable oscillation starts. The frequency of oscillation will vary with load from approximately 100Khz in standby to 38Khz with a full load (120 watts AC input power).

The feedback winding between pins 5 and 7 on T4101 is tightly coupled to the secondary windings. The voltage on the feedback winding will follow the voltage changes on the secondary windings. The voltage developed on pin 7 of T4101 is rectified by CR4111 and filtered by C4127. This negative voltage is applied to pin 1 of U4101. There is a precision voltage reference inside U4101 trimmed to -40.5 volts +/- .5 volts. The error amplifier tries to make the voltage on pin 1 of U4101 equal to the reference voltage. If the load on the secondaries increases and the voltage drops, the voltage developed at pin 7 of T4101 would decrease (less negative). This would allow the FET to stay on longer increasing the output voltage. In this way, the IC is able to hold the output of the supply constant with varying line voltages and loads.

If an excessive load is placed on the power supply outputs, the on time of the FET will increase. This will result in more current through the FET and the source resistor R4124. The voltage drop will be proportional to the current. This voltage will charge C4124 and at some point turn on the OCP circuitry in U4101 causing the FET to turn off. The value of C4124 is critical the OCP trip point.

The network composed of C4122, C4128, R4126 and CR4112 is a snubber network used to reduce the high voltage spike developed when the FET turns off. C4103 and R4105 are part of a compensation network that stabilize the supply from parasitic oscillations. R4129 is an ESD (Electrostatic Discharge) protection resistor for the gate of the FET inside U4101. R4122 and CR4109 help stabilize the OCP circuit against line voltage variations. Ferrite beads in the circuit are for RFI (Radio Frequency Interference) emission reduction. C4107, L4102 and C4105 form a filter network to reduce the ripple in the regulated B+ and reduce high frequency switching noise.

Troubleshooting

1. Measure the voltage on pin 1 of U4101. It should be -40.5 volts +/- 0.50 volts. If it is correct, the IC is probably working. If it is not correct, there is most likely an abnormal load on the power supply. As the output loads increase above the design ratings, the output voltages and the oscillation frequency will drop. If the loads are high enough, the frequency of the power supply will be in the audible range. If there is a short on the secondary of T4101, the supply will shut down until the short is removed. Under normal conditions, a short on the secondary will not damage the supply. Under no load conditions, the regulated B+ will rise and the supply will go into a burst mode where there is a series of burst pulses.
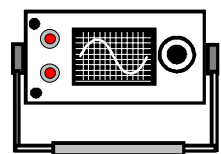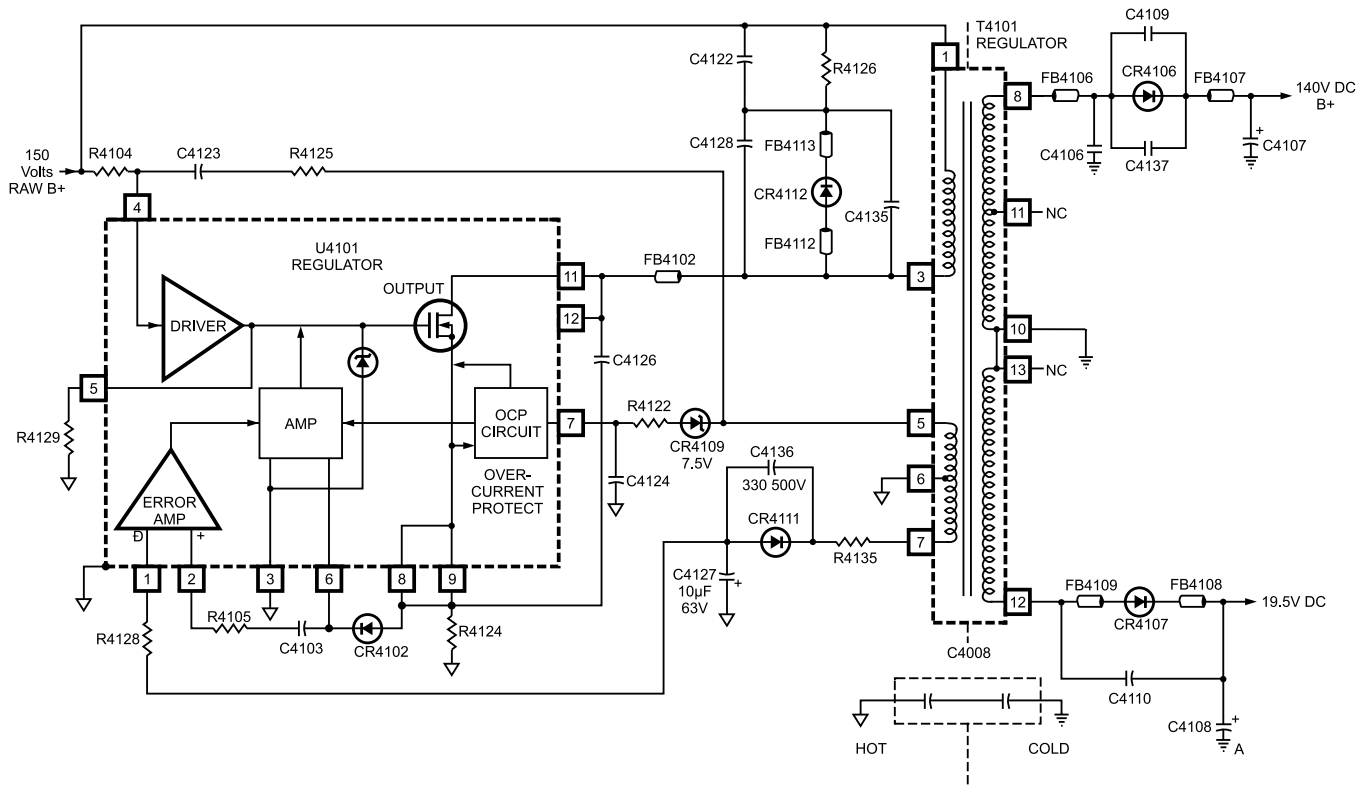
Figure 4, CTC176/177 Power Supply

> **Note: It is not recommended running the supply with no load. The output filter capacitors may be stressed by over-voltage.**

2. If pin 1 of U4101 is shorted, the regulated 140 volt B+ will be low, approximately 30 volts. If pin 1 is open, the regulated 140 volt B+ will rise to over 200 volts.

3. If F4001 blows, U4101 is most likely shorted.

4. If regulated B+ is too low, suspect an excessive output load, defective T4101 or a shorted C4127.

5. If regulated B+ is too high, suspect a no-load condition on the secondary of T4101 or an open in the feedback path to pin 1 on U4101.

   Note: It is normal for the 140 volt supply to rise 4 or 5 volts in the standby mode.

6. If the supply will not oscillate, suspect a defective U4101, T4101, R4104, R4125 or C4123.

7. For poor regulation, suspect a defective T4101, U4101, C4103 or R4105.

Power Supply

The power supply in the CTC175 is a simple series pass regulator with microprocessor controllability. 150 volts raw B+ is applied to the collector of Q4150, an integrated darlington regulator. R4155 passes a portion of the total current around Q4150 to minimize current dissipation in the transistor. The output of the regulator is filtered by C4153.

The feedback loop for the supply begins with a voltage divider made up of R4157 and R4158. The divider feeds the input of a comparator at pin 30 of U1001. A PWM (pulse width modulated) output from pin 28 of U1001 feeds Q4153 inverting the control voltage to the base of Q4151. Q4151 controls the base bias of Q4150. As a load increases on the 140B+ supply, the voltage to pin 30 drops, causing the PWM output from pin 28 of U1001 to increase, forward biasing Q4153 harder. This in turn reduces the base bias to Q4151 increasing the forward bias on Q4150, increasing the B+ output of the power supply.

The PWM circuit inside U1001 is also affected by beam current via the size compensation input pin 16 which is also used in the vertical circuit to minimize raster blooming (see vertical circuit). This helps stabilize the linear regulator during heavy beam current transitions. As beam current increases, regulator output decreases.
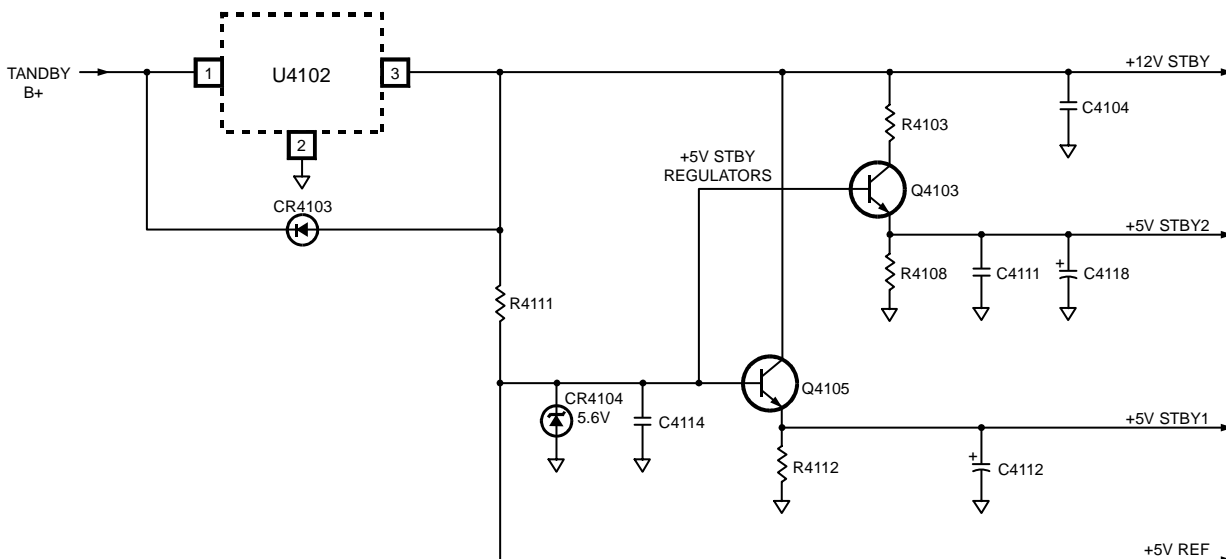

Figure 5, CTC175 Power Supply

Troubleshooting

Failures of the linear regulator can be difficult to detect if the AC line voltage is constant. Using a variac to check proper regulation is the best approach. If the regulator circuit is suspected of being defective, perform the following steps:

1. Apply 105 to 130 VAC to the TV and check the 140 B+ output. If the B+ is not 140 volts, enter the service alignments and attempt to raise and lower the B+ with the digital "B+ Trim" adjustment (parameter #18). If the adjustment has no effect, go to the next step. If the 140 B+ can be set, the circuit is most likely functioning correctly.

2. Monitor the collector voltages on Q4153 and Q4151. The voltages should increase and decrease inversely as the B+ trim adjustment is performed. If this is not the case, suspect Q4153 or Q4151. If the voltage varies with the alignment, but the B+ does not change, suspect a defective Q4150.

T E C H
T I P
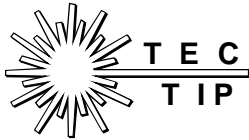
Note: A shorted horizontal output, Q4401, will most likely cause Q4150 to short. Always check Q4150 after replacing a defective Q4401.

Standby Supplies

The standby supplies provide a Standby 12 volt supply, two Standby 5 volt supplies and one 5.6 volt reference supply. Approximately 20 volts, from the switching supply on the CTC176/177 or the standby bridge rectifier on the CTC175, is applied to pin 1 of U4102, a three-legged 12 volt regulator. The output on pin 3 serves as the 12 volt standby supply. The 12 volt supply is also applied to the cathode of CR4104, a 5.6 volt zener diode, that sets up the base bias for Q4103 and Q4105. A portion of the 12 volts is sent to the collectors of the same transistors for the voltage source. The voltage drop across of the base emitter junction of the transistors produces the 5 volt supplies on their emitters.
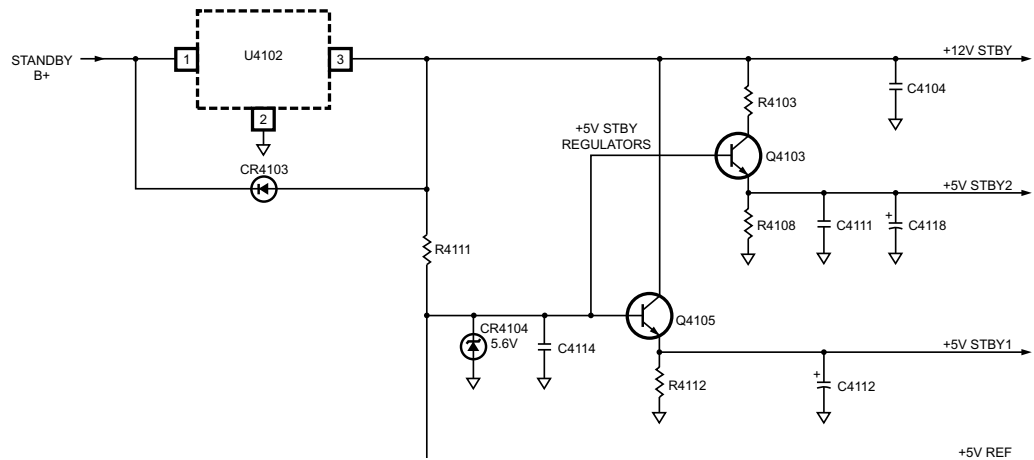

Figure 6, Standby Supplies

Troubleshooting
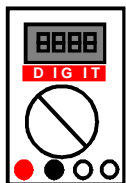
1. Check the 12 volt supply on pin three of U4102.

2. Check the 5.6 volt reference on the cathode of CR4104.

3. Check the 5 volt standby 1 and 2 supplies on the emitter of Q4105 and Q4103 respectively.

The CTC177 chassis family is a digitally controlled television receiver. The system control circuit governs the entire television. The control circuits are not only responsible for turning the set on and off, but also for aligning the different circuits such as deflection and signal. Adjustments once made by adjusting a potentiometer or coil are now performed by reading and writing data to the EEPROM (**E**lectrically **E**rasable **P**rogrammable **R**ead **O**nly **M**emory) using an on-screen menu and the television's remote control.

A newly developed television processing IC, called the T-Chip (Thomson Chip), exchanges information with the system control microprocessor over the serial data bus. This communication is carried out over a three wire bus utilizing the new T-Bus (Thomson Bus) protocol. The T-Chip implements a new level of integration by housing more circuitry than ever before, and reducing the number of external peripheral components.

The system control microprocessor can decode Line 21 closed caption information and display the text on the screen. When implemented, the customer will be able to selectively view the text on closed captioned encoded programs.
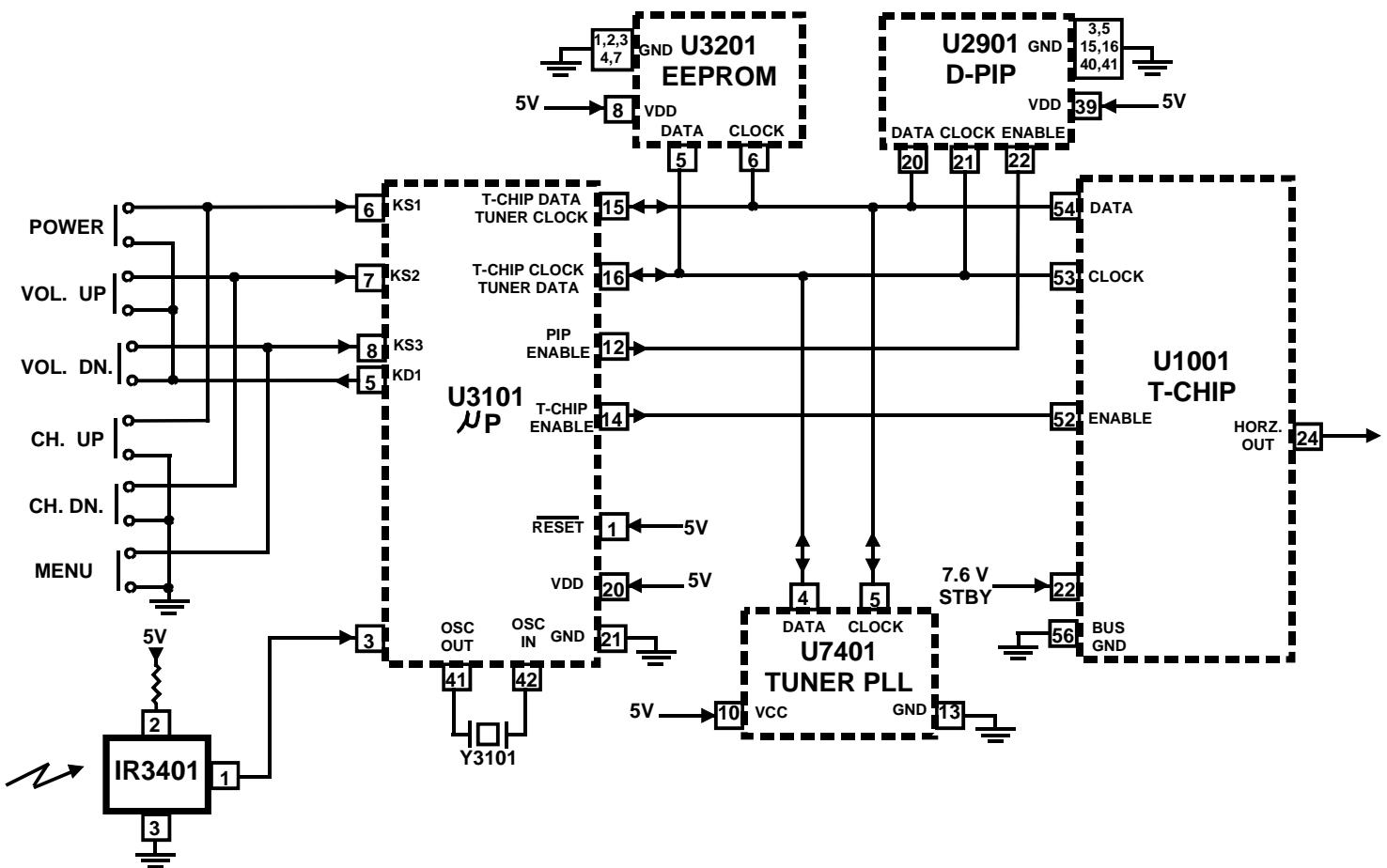
**System
Control**

Figure 7, System Control Block Diagram

Reset Circuit

The reset circuit starts the microprocessor at a known place in its program. U3101 reset is an active low to pin 1. When AC power is first applied, the reset circuit goes high after approximately 55msec. This allows the crystal oscillator time to come up and stabilize before allowing the microprocessor to run. The reset circuit also monitors the condition of the 12 volt standby supply. If the 12 volt standby supply drops below 10 volts, the reset circuit activates and puts the microprocessor in a low power mode.
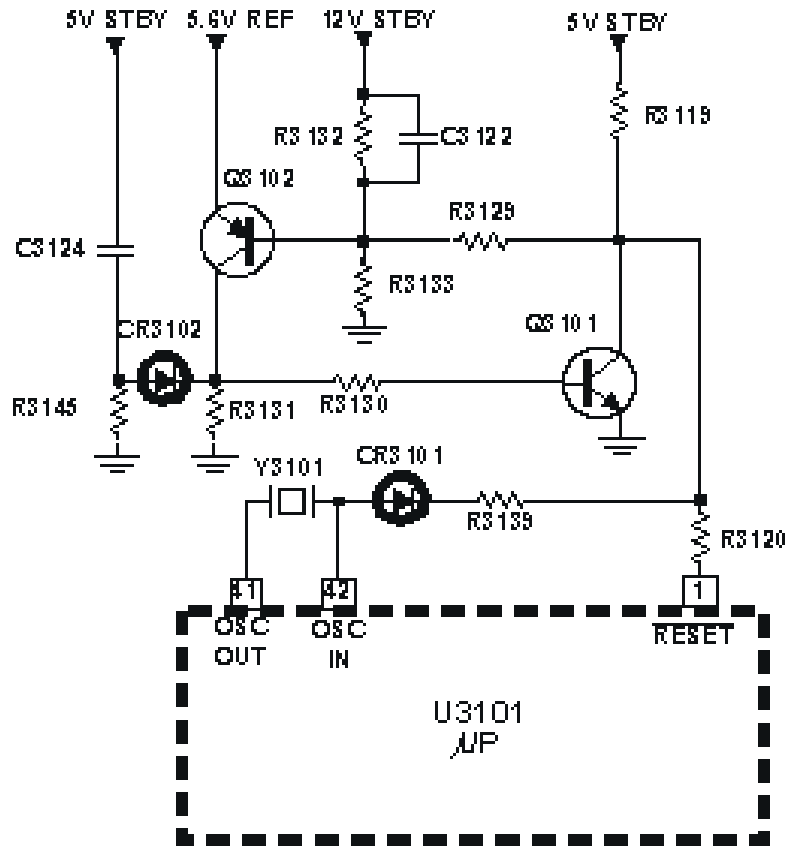
Figure 8, Reset Circuit

A stable 5.6 volt reference is applied to the emitter of Q3102. The 12 volt standby supply is divided by R3132 and R3133 so approximately 6 volts is applied to the base of Q3102. The collector of Q3102 is tied to the base of Q3101. The collector of Q3101 is connected to the 5 volt standby supply and to the reset pin 1 of U3101. Under normal operating conditions, the voltage on the base of Q3102 is at 6 volts which is high enough to keep Q3102 off. If the 12 volt standby supply drops far enough to allow the voltage on the base of Q3102 to drop to 5 volts, Q3102 will turn on. When Q3102 turns

on, Q3101 will also turn on and disable the 5 volt reset line to ground initiating a reset to U3101. Q3101 also disables the crystal oscillator by grounding it through R3139 and CR3101. This places the microprocessor in a low power mode to maintain the non-volatile memory.
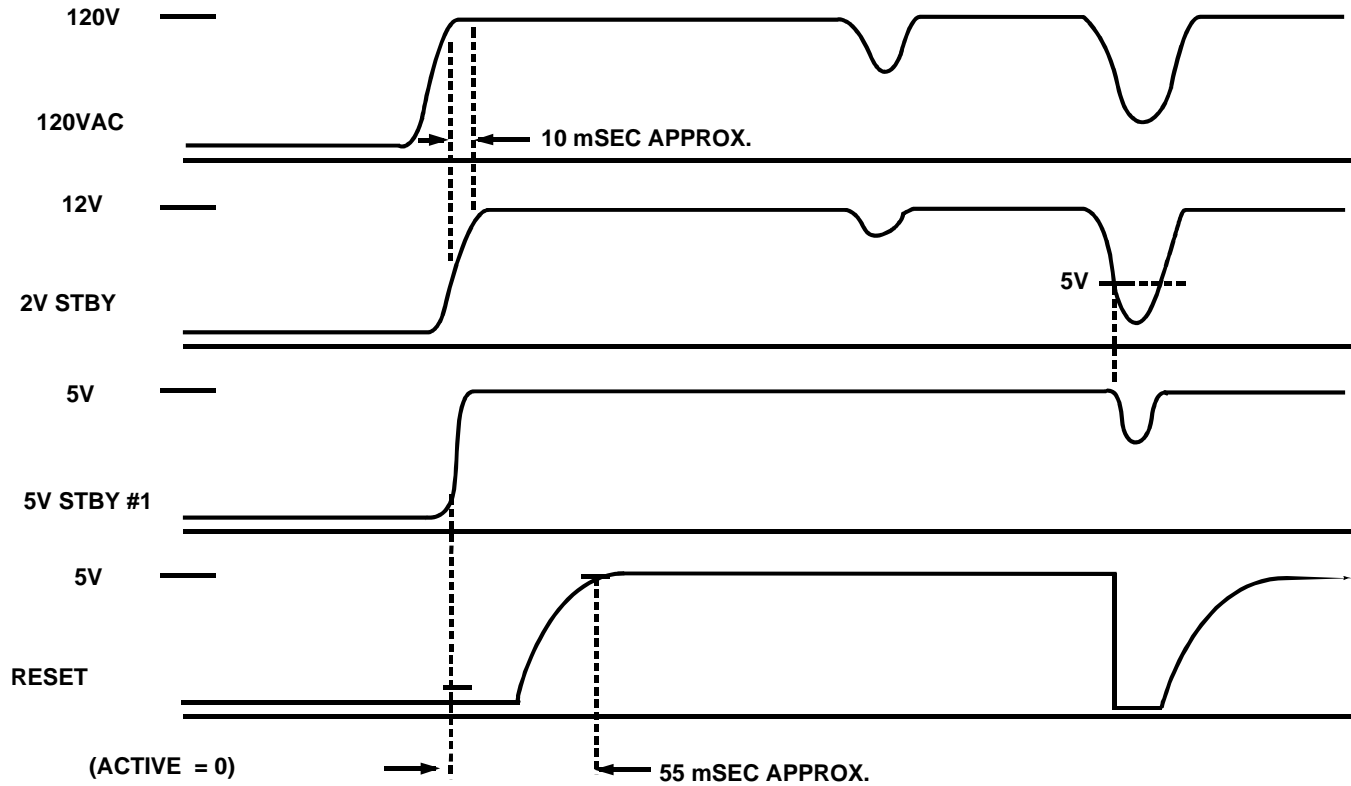
Figure 9, Reset Circuit Timing

Data Communications

Five IC's make up the system control circuit: U3101, main microprocessor; U1001, T-Chip; U2901, D-PIP microprocessor; U3201, EEPROM; and U7401, tuner PLL(Phase Lock Loop). These IC's communicate with U3101 via serial data lines. The format used to communicate is called "bus protocol." Three bus protocols are used in this system: IM Bus, I²C Bus and the T-Bus. While it is not necessary for the technician to completely understand the individual protocols for troubleshooting the system control circuits, knowing what type of information is exchanged and what IC pins are involved will make troubleshooting more efficient and effective. All circuits in the CTC177 chassis family interface with the system control circuit in one form or another. It is important to decide whether the circuit itself is at fault or if the system control circuit is the problem.
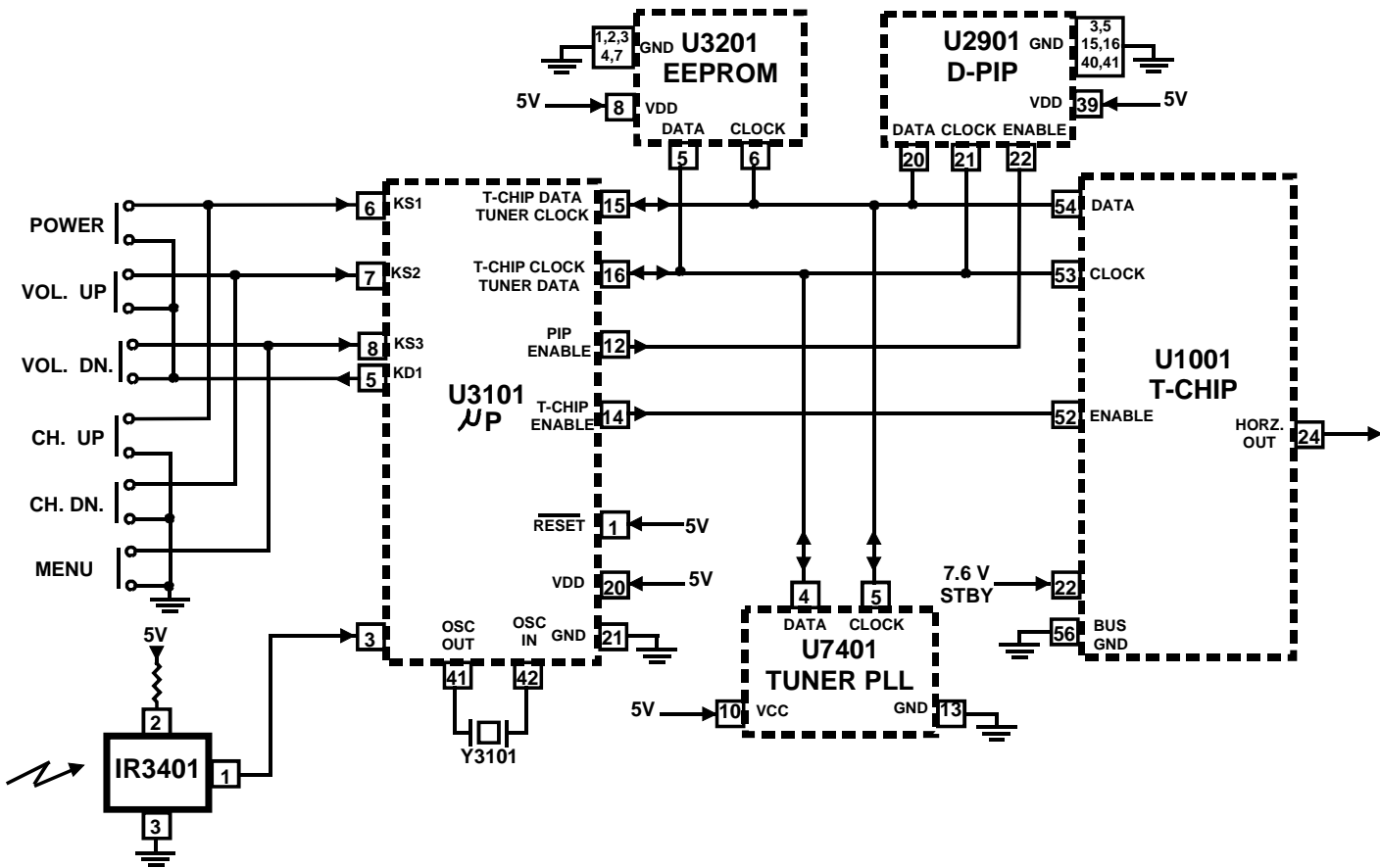
Figure 10, System Control Circuit (repeated)

IM Bus

The IM Bus is a three wire bus U3101 uses to communicate with the D-PIP microprocessor. Pins 15, 16 and 12 on U3101 are the IM Bus Data, Clock and PIP Enable lines. These are connected to pins 20, 21 and 22 respectively on U2901, the D-PIP microprocessor. When the PIP Enable line goes low, eight bits of address data synchronized to clock transitions are sent. Next, the Enable line goes high followed by eight bits of "Write" or "Read" information. The Enable line then momentarily goes low to signal the end of the transaction. Because the PIP Enable line and data protocol are unique to the PIP microprocessor, other devices that share the data and clock lines are unaffected by communications between U3101 and U2901.

I²C Bus

The I²C Bus is a two wire bus U3101 uses to communicate with the tuner PLL, U7401 and EEPROM, U3201. Pins 15 and 16 of U3101 are the clock and data lines for the I²C Bus. Notice this is reversed compared to the IM Bus. These pins are connected to pins 6 and 5 of U3201 and pins 5 and 4 of U7401 respectively. Data transfers are signaled when the data line goes LOW while the clock is HI. Eight bits of address data followed by an acknowledge bit are sent. Next, eight bits of Read/Write data followed by an acknowledge bit are sent. Because the data protocols are unique and the enable lines are not used, only I²C Bus devices respond to I²C Bus commands.

T-Bus

The T-Bus protocol is a three wire bus enabling U3101 to communicate with U1001. This bi-directional bus allows the microprocessor to control the operations within U1001 and allows U1001 to report operation status back.
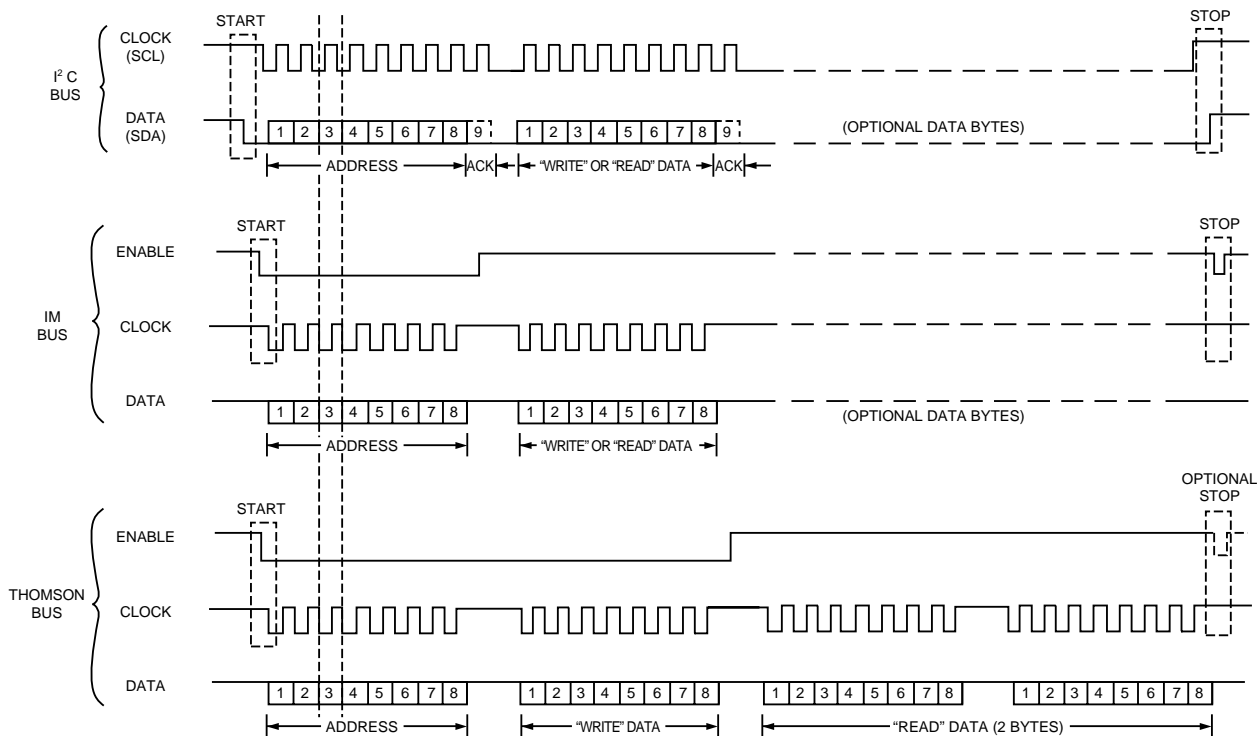
Figure 11, Bus Protocols

Two distinct sections of a T-Bus transaction are called Read and Write. During the Write portion, the microprocessor drives the DATA line to send new register information to U1001. During the Read portion, U1001 drives the DATA line to transfer status information to the microprocessor, U3101.

The Write portion of the transaction is 16 bits long consisting of an IC Address (4 bits), Subaddress (5 bits) and Data field (7 bits). The Address identifies U1001. The Subaddress indicates the register inside U1001 and the Data is the value of the information being sent to U1001 by U3101. The Write portion of the transaction begins when U3101 pulls the ENABLE line low. Once the ENABLE line is low, the microprocessor must drive the DATA line one bit at a time while toggling the clock line. U1001 accepts data on the rising edge of the clock pulse.
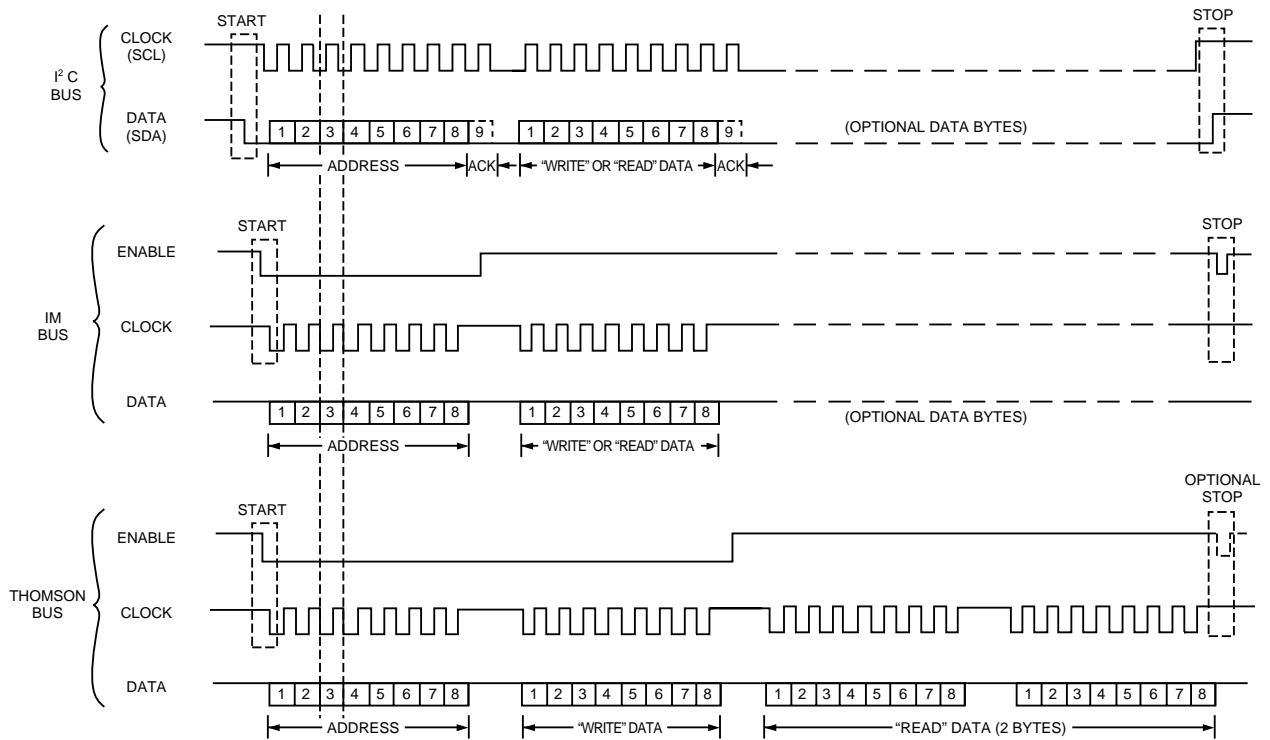
Figure 12, Bus Protocols (repeated)

After the Write portion of the transaction is completed, the Read portion begins. The Read portion is the answer back to U3101 from U1001. It too is 16 bits long consisting of Acknowledge (4 bits), Status (4 bits) and Data (8 bits). The Acknowledge bits let U3101 know it did in fact access U1001. The Status bits S0 through S3 inform U3101 of operating conditions in U1001:

S0 - Power-ON-Reset (POR)

S1 - X-ray Protection Fault (XRP)

S2 - Horizontal Lock Detector

S3 - Delayed Transfer Complete (BID)

The last 8 bits of the Read portion contain the Digital AFT information from the IF. This information is only looked at during channel change.

POR (Power-ON-Reset)

U1001 has a standby power monitor called POR. This circuit detects when the Standby Vcc has dropped below approximately 6 volts and shuts the IC off by stopping both the PWM and horizontal outputs. The output of the POR circuit is available to U3101 as one bit every T-Bus transaction.

The POR circuit output is latched and reset on the OFF to ON transition of the ON/ OFF bit. This means when the TV is ON and a standby transient occurs that triggers the POR circuit, it is necessary to send an OFF command followed by an ON command to get the set started again. If the Standby Vcc is still too low when an ON command is received, the IC will stay in the OFF mode requiring the process to be repeated.

XRP

The XRP bit in the status portion of the T-Bus transaction informs U3101 if an XRP condition has occurred. When the XRP input is above the reference value, the comparator's output will turn the TV off by stopping both the PWM and Horizontal outputs.

The XRP bit is latched internally and gets reset at the ON to OFF transition of the ON/ OFF bit. This means to restart the TV after an XRP trip, the microprocessor must first send an OFF command followed by an ON command.

When the ON/OFF bit is in the OFF state, the XRP latch is disabled internally. This means for U3101 to read the valid state of the XRP detector, it is necessary for the ON/ OFF bit to be in the ON state.

Horizontal Lock Detector

This detector compares the position of the flyback pulse with the sync of the selected video source. This output is available to the microprocessor as a bit on the Read portion of every T-Bus transaction. While this detector can be used to detect the presence of an active channel, it is not used for tuning. A separate sync pulse input is applied to pin 39 of U3101 for that purpose.

The horizontal lock detector is used for detecting whether or not an active video source is connected to the composite or s-video input jacks. When s-video or composite video is selected, U3101 selects the video source and looks at the horizontal lock bit. If lock is detected, the source appears on the screen. If no lock is detected, U3101 displays "UNUSABLE SIGNAL" on the screen.

The horizontal lock bit also informs U3101 whether or not to select s-video or composite video. When "00" is entered to select a video source, U3101 first selects s-video and checks for a lock. If no lock occurs, composite video is selected.

Delayed Transfer Mode (BID)

This bit is used in transferring of data to the T-Chip registers. It is currently not used.

Power-On Sequence

U3101 does not have a single on/off control pin to turn the television on or off as in previous chassis. The T-Chip is controlled entirely via the serial bus. Power on/off commands are accomplished by U3101 telling U1001 to turn on horizontal drive by means of a data command. U1001 contains its own standby 7.6 volt regulator to keep data communications alive and the horizontal drive stage operative while the set is off (Standby Mode). When the On command is received and horizontal drive is established, run supplies come up and bias the rest of U1001's circuits bringing the set into the full on mode. An Off command from U3101 will cause horizontal drive to cease resulting in the scan derived supplies turning off. This removes power to the other circuits associated with U1001, placing the set in the standby mode.
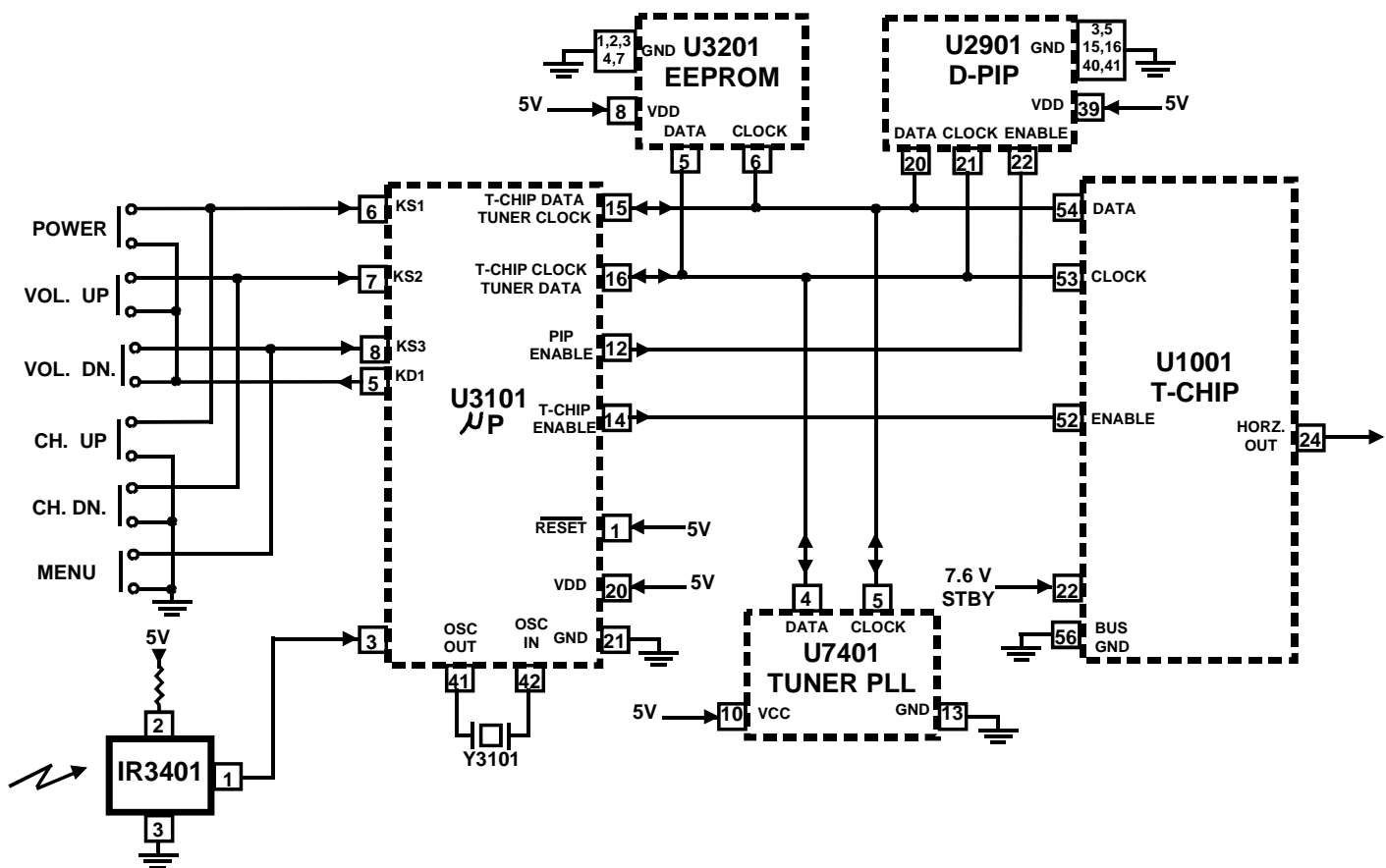
Figure 13, System Control Circuit (repeated)

U3201 is the **E**lectrically **E**rasable **P**rogrammable **R**ead-**O**nly **M**emory and uses the I²C Bus DATA and CLOCK lines to communicate with U3101. It provides non-volatile memory for storing the following:

U3201 - EEPROM

- Channel Scan List

- Customer Features

- Chassis Alignments

- CRT Alignments

- DPIP Alignments

- Tuner Alignments

- Channel Labels

If for any reason the EEPROM is replaced, the television will have to be completely realigned to store the correct alignment data in the new chip. For this reason, it is important not to change U3201 unless it is absolutely necessary.

TECH TIP
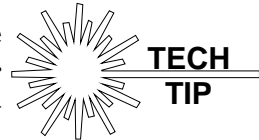
The keyboard interface is very similar to those used in the past. An important difference is only one key drive line, KD1, is used. POWER, VOL. UP and VOL. DN. are driven by KD1. When one of these buttons is pressed, KD1 pulses the corresponding sense line low. U3101 detects which button has been pressed by monitoring the sense lines for the KD1 pulse. The other three switches pull KS1, KS2 and KS3 to ground. When U3101 sees a constant LO instead of a HI to LO pulse, it knows one of the other three buttons has been pressed and will initiate the appropriate function based on which sense line is pulled low.

Keyboard Interface

Infrared remote signals are amplified by IR3401 and appear at U3101 pin 3 as 5 Vpp data pulses. When no IR is received, the DC level at U3101 pin 3 is 5 volts. IR3401 is powered by the 5 volt standby supply.

IR Input

Figure 14, Non-Closed Caption, Early Production OSD Circuit

Two OSD circuits are used in the CTC177 chassis family. Early production televisions that do not support a closed caption decoder have a cyan OSD. Later production sets that include a closed caption decoder have a full color OSD.

On Screen Display

Early production sets with a cyan display use only one OSD line out of U3101 to drive the green and blue OSD input on U1001. The OSD is produced in U3101 and is output from pin 18. Q2701 buffers the signal and capacitively couples it to the green and blue input on U1001 pins 41 and 42. Green and blue are driven equally resulting in the cyan display.
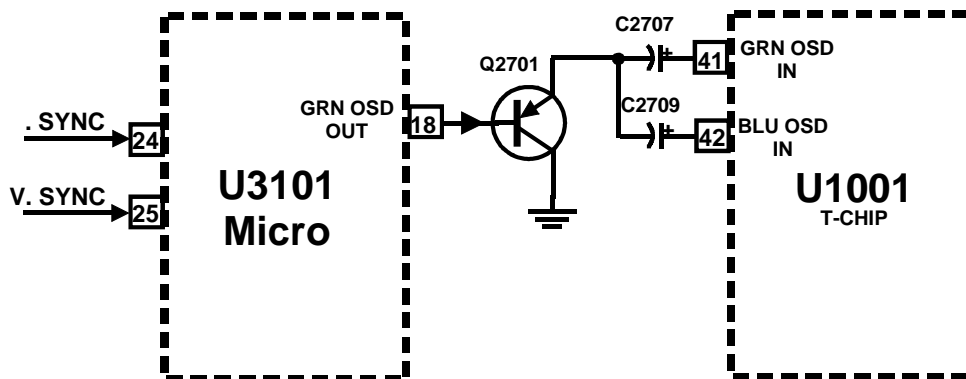
Later production sets that support closed caption decoders use red, green and blue outputs from U3101 (pins 19, 18 and 17) to drive the red, green and blue OSD inputs on U1001 (pins 40, 41 and 42) producing a full color OSD. Q2702, Q2701 and Q2703 buffer the red, green and blue signals and capacitively couple them to pins 40, 41 and 42 of U1001 respectfully.

Horizontal and vertical sync are input to pins 24 and 25 of U3101 and are used to control the position of the OSD on the screen.
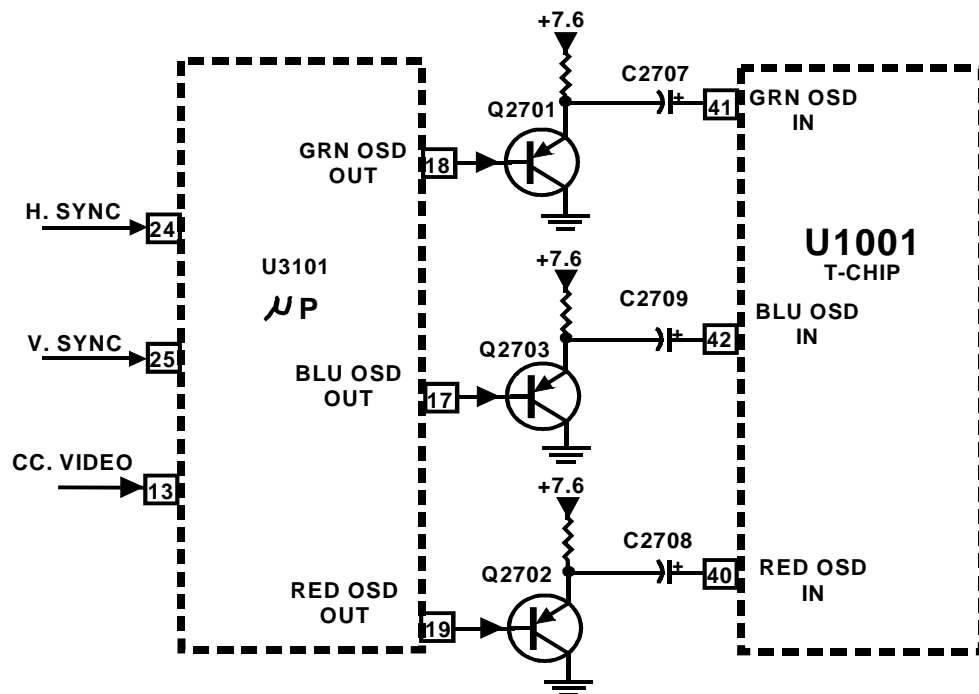
Figure 15, Closed Caption OSD Circuit

Closed Caption

U3101 contains a closed caption decoder that interprets the closed caption data sent on line 21 of the first field in each frame of video. Sets that support the closed caption feature, video is input to pin 13 of U3101. The closed caption signal begins with a seven cycle burst of pulses to synchronize the decoder's data clock. This is followed by a start bit followed by two eight-bit words consisting of seven bits of data followed by a parity bit for error correction. Since two characters are sent on line 21 of the first field of each frame, there are a total of 60 characters per second. This format sends two data channels called C1 and C2 (caption channel 1 and caption channel 2). Channel 1 is used for the main captioning text while channel 2 is used for alternate text, such as a second language or abbreviated captioning for children or slow readers. C1 and C2 are selectable from the menu; however, the TV will default to C1 each time the TV is unplugged for prolonged periods of time.

All closed caption processing is performed inside U3101. Horizontal and vertical sync at pins 24 and 25 of U3101 are also used by the closed caption decoder.
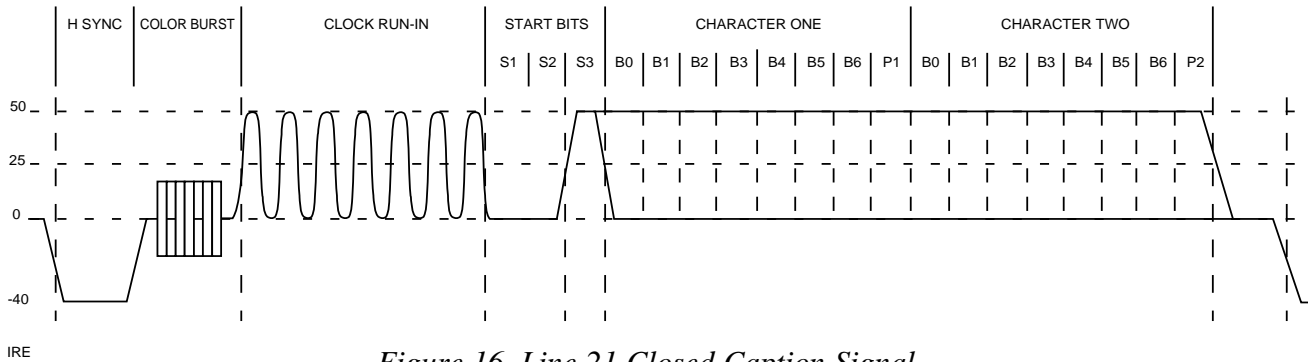
Figure 16, Line 21 Closed Caption Signal

Service Menu

The service menu provides a method for instrument alignment and setup. This mode is accessed by pressing two combinations of buttons on the front panel keyboard. With the instrument on, press and hold the *menu* button and then simultaneously press the *power* button. While continuing to hold the *menu* button, release the *power* button and then press the *volume +* button. The instrument should immediately display a one line menu on the screen:
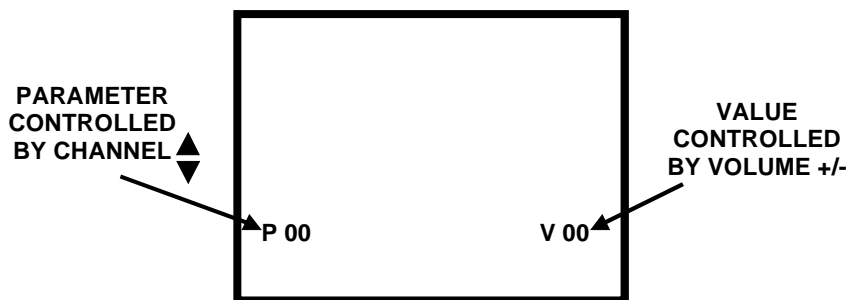
Figure 16, Service Menu

The decimal value on the left is the parameter number and the decimal value on the right is the current value of that parameter. Channel up and down increment and decrement the parameter number. Volume + / - adjust the current value of that parameter. Three parameters are used for security purposes to protect the factory alignments from being modified by the customer. The first security parameter, 00, requires a specific value to be selected with the volume +/- buttons before other parameters may be selected. If channel *up/down* is pressed without the correct security pass-number set, the service mode is exited. There are three main groups of parameters: instrument parameters, chassis parameters, and tuner parameters. The chassis and tuner parameters are each preceded by a security pass-number parameter to make changes very deliberate.

Most of the instrument and chassis parameters correspond to individual (unpacked) register fields in the T-chip. When these parameters are modified, the T-chip and the corresponding EEPROM location is updated.

The Menu button may be used to enable the vertical collapse setup line - it functions as a toggle. This setup line has the following characteristics:

- S-video source is automatically selected (make sure no signal is connected to the S-video input)

- Contrast is set to minimum

- Brightness is set to 7.5 IRE

- Vertical kill enabled

When the setup line is toggled off, the characteristics modified above return to their prior settings except contrast which is set to the factory default. Changing to another parameter (with channel up/down) also toggles off the setup line.

The tuner parameters correspond to the three alignments for each of 19 channels for a total of 57 parameters. When these parameters are modified, the tuner D/A and the EEPROM are updated. Note that you must manually select the proper channel for each tuner alignment. These adjustments may be made from the front panel as well as the remote. The digit entry buttons (on the remote) allow tuning to any channel in this mode. Pressing the power on, off, or power toggle buttons exits this service mode.

Alignment
Parameters

SERVICE MENU CHART

Parameter # Chan to Change	Parameter Name	Value Range Vol to adjust	Comment:
00	Pass No. for Serv. adjust	Must set to 76	May not advance until value set

Service Adjustment Parameters

01	Horiz. Freq.	00-31	sync is killed
02	Horiz. Phase	00-15	
03	EW DC (width)	00-15	27″ only
04	EW Amplitude	00-07	27″ only
05	Vertical DC	00-15	
06	Vertical size	00-31	
07	Red Bias	00-127	press Menu button for setup line
08	Green Bias	00-127	press Menu button for setup line
09	Blue Bias	00-127	press Menu button for setup line
10	Red Drive	00-63	press Menu button for setup line
11	Green Drive	00-63	press Menu button for setup line
12	Blue Drive	00-63	press Menu button for setup line
13	Security pass no. for chassis align parameters	Must set to 77	may not advance to higher param. until value set

Chassis Alignment Parameters

14	PLL Tuning	00-63	
15	4.5 MHz Trap	00-07	
16	Video Level	00-07	
17	FM Level	00-15	
18	B+ Trim	00-15	CTC175 only
19	RF AGC Chan 6	00-31	Man. tune chan 6
20	RF AGC Band 1	00-31	Man. tune Band 0 channel 17
21	RF AGC Band 2	00-31	Man. tune Band 2 Channel 50
22	RF AGC Band 3	00-31	Man. tune Band 3 Channel 125
23	D-PIP Chroma		
24	D-PIP tint		
25	D-PIP bright		
26	D-PIP contrast		
27	Factory tint	00-63	
28	Security pass No. for tuner align.	Must set to 78	May not advance to higher param. until val. is set

VCR-Used as signal source for tuner service modulator.

DVM-Digital volt meter.

External DC Power Supply-Voltage source to power service modulator.

The entire electronic tuner alignment procedure, once started, *must* be completed in it's entirety. Electronic Tuner Alignment is performed with top & bottom tuner covers in place with bottom cover soldered.

Electronic Tuner Alignment Parameters

Parameter # Chan to Change	Parameter Name	Value Range Vol to adjust	Parameter # Chan to Change	Parameter Name	Value Range Vol to adjust
100	Ch. 2 secondary	00-63	128	Ch. 50 primary	00-63
101	Ch. 2 primary	00-63	129	Ch. 50 single	00-63
102	Ch. 2 single	00-63	130	Ch. 51 secondary	00-63
103	Ch. 6 secondary	00-63	131	Ch. 51 primary	00-63
104	Ch. 6 primary	00-63	132	Ch. 51 single	00-63
105	Ch. 6 single	00-63	133	Ch. 57 secondary	00-63
106	Ch. 14 secondary	00-63	134	Ch. 57 primary	00-63
107	Ch. 14 primary	00-63	135	Ch. 57 single	00-63
108	Ch. 14 single	00-63	136	Ch. 63 secondary	00-63
109	Ch. 17 secondary	00-63	137	Ch. 63 primary	00-63
110	Ch. 17 primary	00-63	138	Ch. 63 single	00-63
111	Ch. 17 single	00-63	139	Ch. 76 secondary	00-63
112	Ch. 18 secondary	00-63	140	Ch. 76 primary	00-63
113	Ch. 18 primary	00-63	141	Ch. 76 single	00-63
114	Ch. 18 single	00-63	142	Ch. 83 secondary	00-63
115	Ch. 13 secondary	00-63	143	Ch. 83 primary	00-63
116	Ch. 13 primary	00-63	144	Ch. 83 single	00-63
117	Ch. 13 single	00-63	145	Ch. 93 secondary	00-63
118	Ch. 34 secondary	00-63	146	Ch. 93 primary	00-63
119	Ch. 34 primary	00-63	147	Ch. 93 single	00-63
120	Ch. 34 single	00-63	148	Ch. 110 secondary	00-63
121	Ch. 37 secondary	00-63	149	Ch. 110 primary	00-63
122	Ch. 37 primary	00-63	150	Ch. 110 single	00-63
123	Ch. 37 single	00-63	151	Ch. 117 secondary	00-63
124	Ch. 48 secondary	00-63	152	Ch. 117 primary	00-63
125	Ch. 48 primary	00-63	153	Ch. 117 single	00-63
126	Ch. 48 single	00-63	154	Ch. 125 secondary	00-63
127	Ch. 50 secondary	00-63	155	Ch. 125 primary	00-63
			156	Ch. 125 single	00-63

The system control circuit controls every function of the TV. A failure in this circuit will cause the entire TV to malfunction. Because U3101 and U1001 are so interrelated, there is a lot of overlapping in troubleshooting procedures. A failure of U3101, U1001, U3201, U2901 or U7401 can make the television completely inoperative. It is important to follow a systematic isolation approach to localize the problem. Because U3101 turns the TV *ON* via a serial data bus command to U1001, a failure in the system control circuit can result in a DEAD SET condition.

System Control Troubleshooting
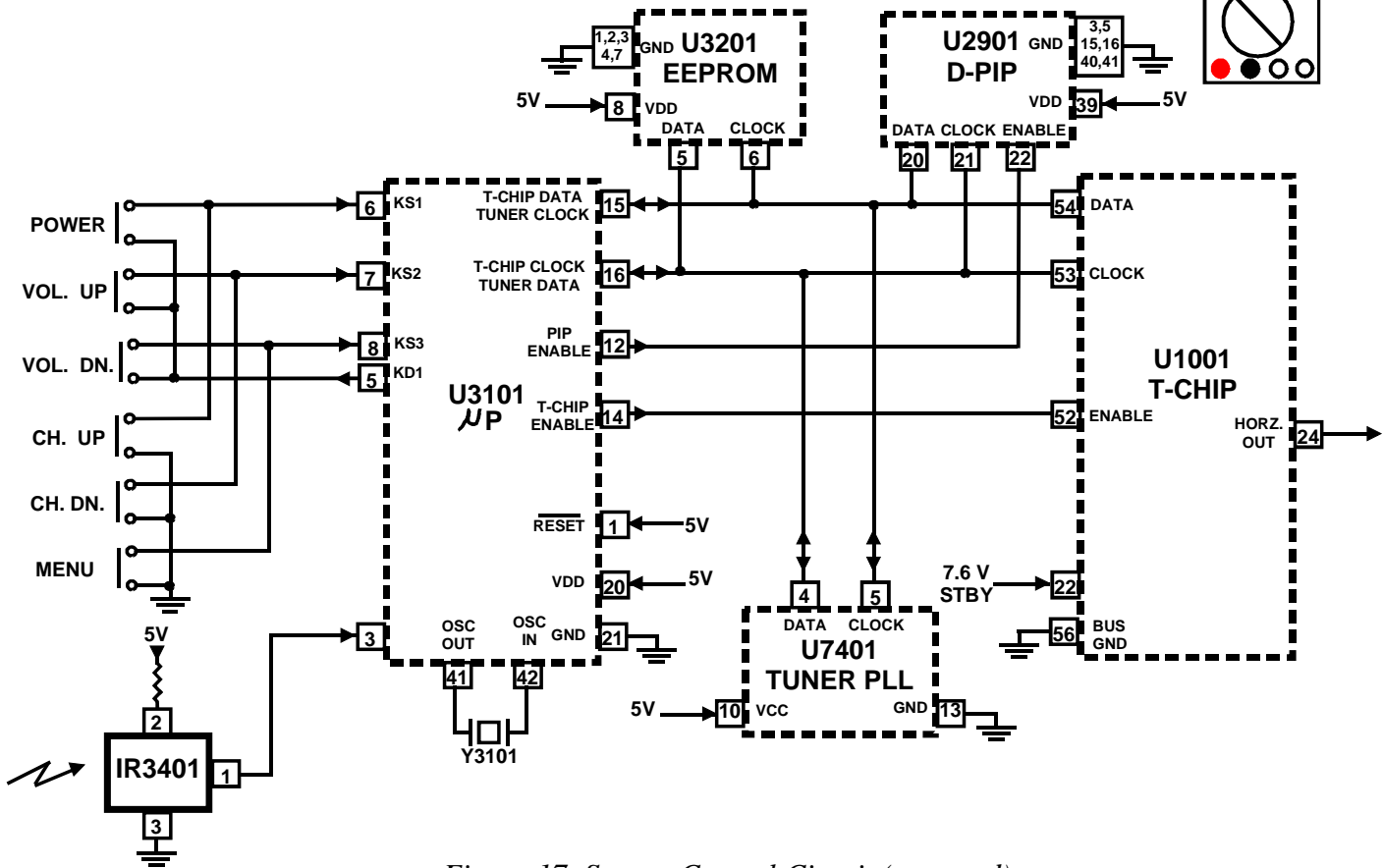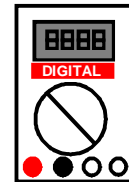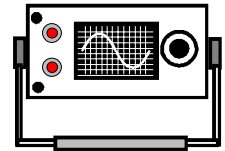
Figure 17, System Control Circuit (repeated)

Dead Set

1. Make sure the standby power supplies are working. (12, 7.6 & 5)

2. Check for horizontal drive pulses out of pin 24 of U1001 when the power button is pressed. If the pulses are there *even momentarily*, system control is working and the problem is in the deflection circuits. If the pulses do not appear, check the 7.6 volt standby voltage on pin 22 of U1001. If the supply is not present on pin 22, unsolder the pin and see if the supply comes up on the pad. If it does, U1001 is defective. If it does not, trace the supply back to its source. If 7.6 volts is present on U1001 pin 22 in circuit, go to the next step.

3. Check for standby 5 volts on pin 20 of U3101. If it is missing, check the power supply. If present, go to the next step.

4. Check the reset pin 1 of U3101 for 5 volts. If it is low or missing, check the reset circuit. If it is, go to the next step.

5. Check pins 41 and 42 of U3101 for a 5 Vpp oscillator. If the signal is not 5 Vpp, check Y3101 and its peripheral components. If the signal is completely absent, suspect U3101 or Y3101. If the 4 MHz signal is present, go to the next step.

6. Monitor pins 14, 15 and 16 of U3101. There should be no data activity in the standby mode. When the power button is pressed, 5 Vpp data pulses should appear. If no pulses appear when the power button is pressed, unsolder pins 20, 21 and 22 of U2901 and pins 4 and 5 of U7401. Now re-check U3101 pins 14, 15 and 16. If data activity returns, suspect a defect in U2901's or U7401's circuit areas. If data activity does not return, go to the next step.

7. Unsolder pins 14, 15 and 16 on U3101 and check for constant 5 Vpp data pulses in the standby mode on those pins.

TECH TIP
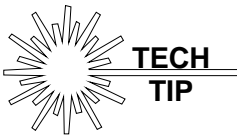
Note: When U3101 is initialized, it checks to see if U3201 is present. Under normal conditions, it immediately finds U3201 and ceases data activity. With the enable, data and clock lines disconnected, U3101 continues to send out data activity looking for U3201. This is normal and indicates U3101 is working.

If no data activity is seen on U3101 pins 14, 15 and 16 with the pins out of circuit, U3101 is probably defective. If data activity is present, reconnect the pins and go to the next step.

8. Having confirmed data activity on pins 14, 15 and 16 of U3101 out of circuit, disconnect pins 5 and 6 of U3201. Check for data activity in the standby mode on the circuit board foil side of U3201 pins 5 and 6. If data activity is present on the foil pads for those pins with the IC out of circuit, U3201 is defective.

TECH TIP

Do not throw away the original U3201 until the problem is absolutely confirmed. If U3201 turns out not to be the problem, putting the old IC back in will prevent a complete chassis alignment from having to be performed.
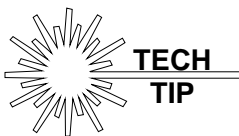
If no data activity is seen on the circuit board with U3201 out of circuit, connect the IC and go to the next step.

9. Unsolder pins 52, 53 and 54 on U1001. Check to see if the data pulses are present on the foil that leads to the pins. If data pulses are present on the circuit board foil, U1001 is most likely defective. If no data pulses appear on circuit board foil side of U1001 pins 52, 53 and 54, suspect an open connection or resistor, or possibly a leaky capacitor on the data bus.

10. Once the problem is isolated and repaired, do not forget to re-connect U2901, U7401 and any other parts that may have been unsoldered during troubleshooting.
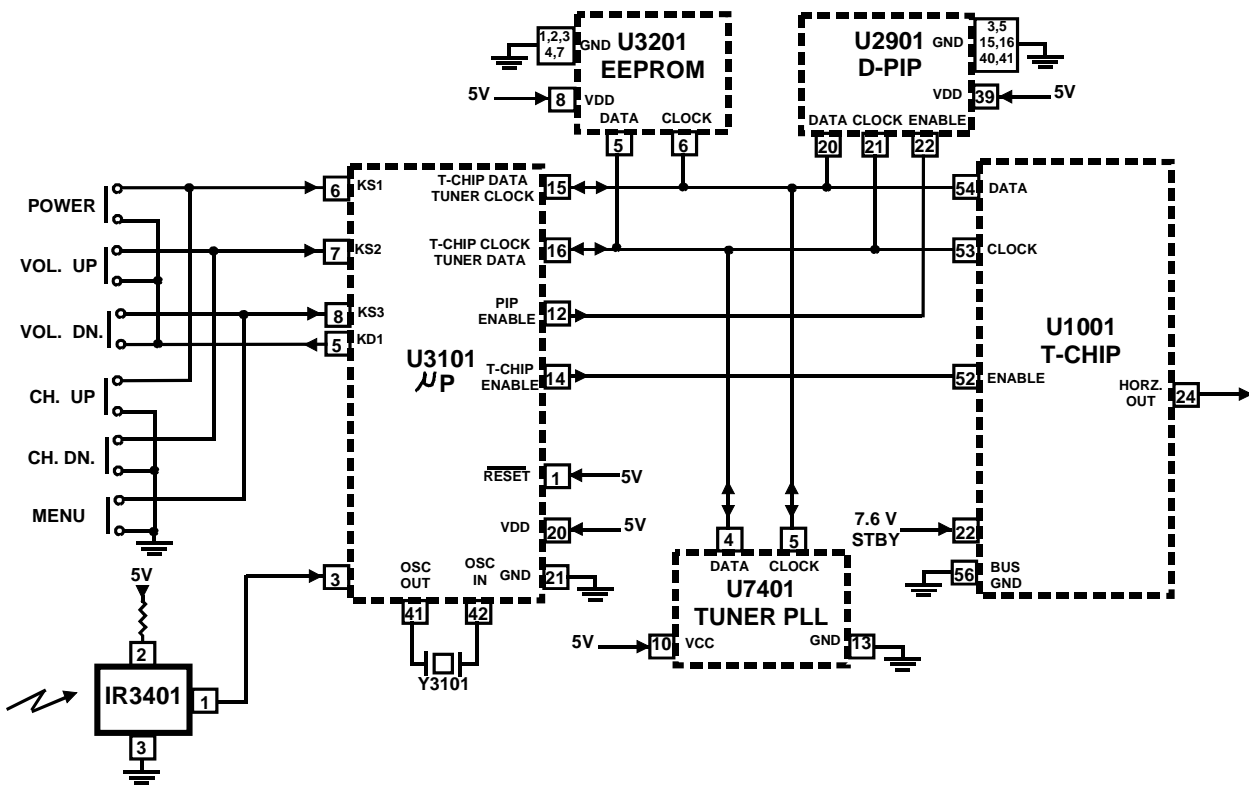
Figure 18, System Control Circuit (Repeated)

Horizontal Deflection

The horizontal deflection circuitry is responsible for generating a current ramp through the horizontal windings of the yoke to deflect the electron beam from left to right. In addition, the horizontal output circuitry generates the high voltage necessary to bias the CRT.

U1001 (T-Chip) performs low level horizontal processing. The functions performed in U1001 are very similar to previous chassis such as the CTC149. The difference is the functions are controlled via the serial data bus. The horizontal processing circuits contained in U1001 are:

- Horizontal Automatic Frequency Control (AFC)
- Horizontal Automatic Phase Control (APC)
- Horizontal Drive
- East West (EW) Pincushion Correction
- X-ray Protection
- Horizontal Vcc Standby Regulator
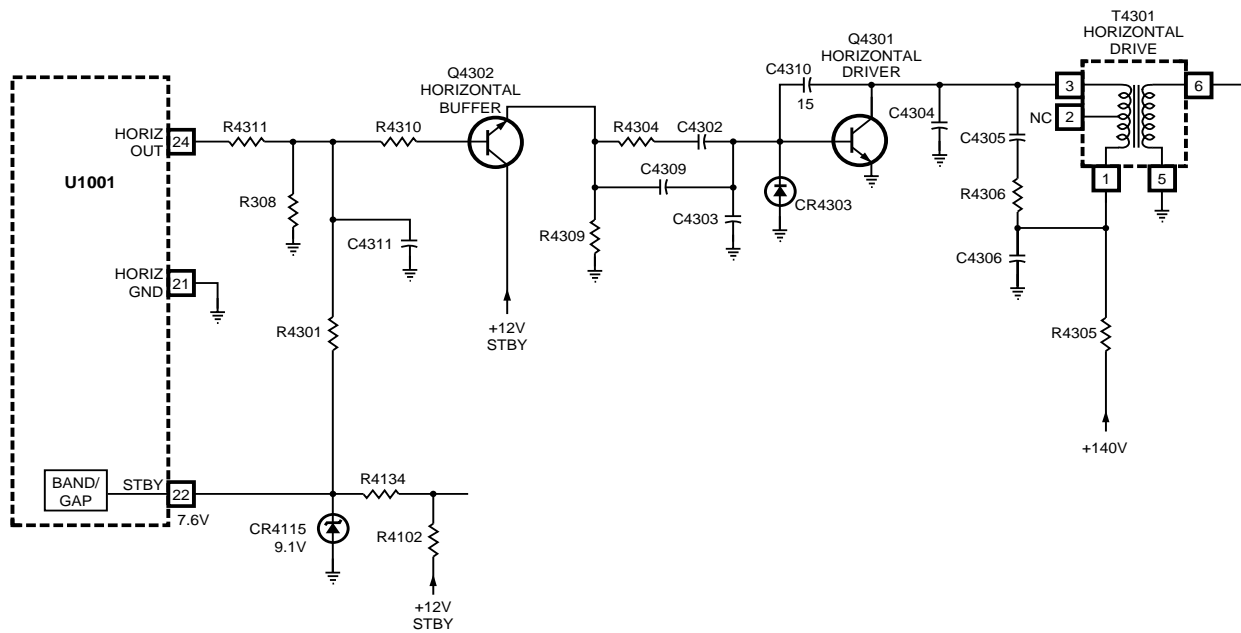
Figure 19, Horizontal Drive Circuit

The horizontal drive and output circuits are conventional in design. The horizontal drive section of U1001 is similar to the CTC149. The output at pin 24 is an open collector that is low (on) when horizontal drive is on. The pulse width is adjustable from 32μsec to 36μsec via serial bus commands to T-Chip register H. Duty (Horizontal Duty). This is set at the factory and is not adjustable in the field.

Q4302 is the horizontal drive buffer that capacitively couples the drive signal to the horizontal driver Q4301. Q4301 drives the primary of T4301, the horizontal drive transformer, to provide the current step-up needed to produce about 1 amp of base drive to the horizontal output transistor, Q4401.
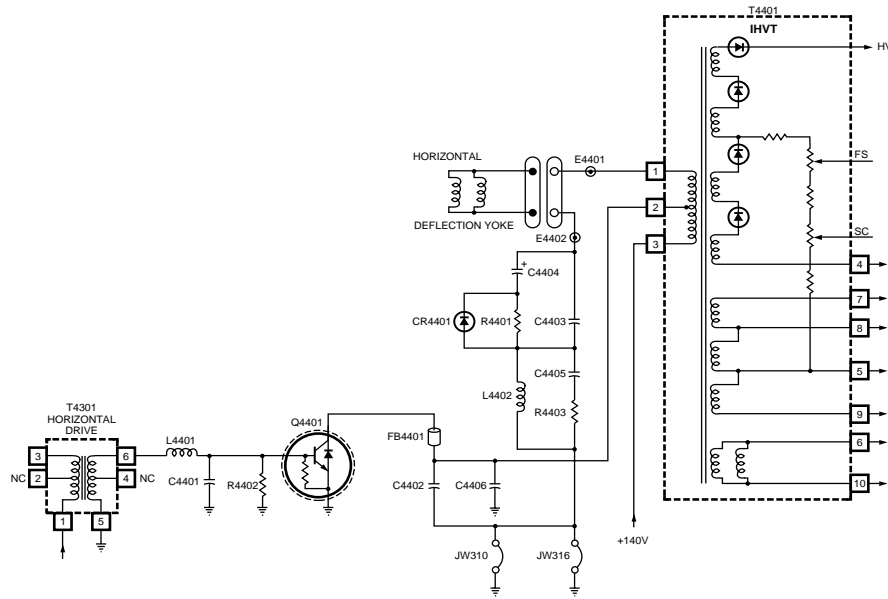
Figure 20, 20" and 25" Horizontal Output Circuit

In 25" and smaller sets, Q4401 is an integrated transistor/damper diode package. 27" and larger sets have a separate output transistor and damper diode which are utilized to allow the use of a diode modulator for pincushion correction. The transistors are NOT interchangeable. The collector of Q4401 is connected to pin 2 of T4401, the IHVT. The 140 volt B+ is input on pin 3 and the horizontal yoke is connected to pin 1 of T4401. The switching action of Q4401 will cause the yoke and retrace capacitor, C4402, to resonate creating a 1000 Vpp retrace pulse. The retrace pulse induces a voltage in the secondary of the IHVT to create the high voltage and scan derived power supplies. The electron beam is scanned across the screen by the resulting current sawtooth through the yoke.
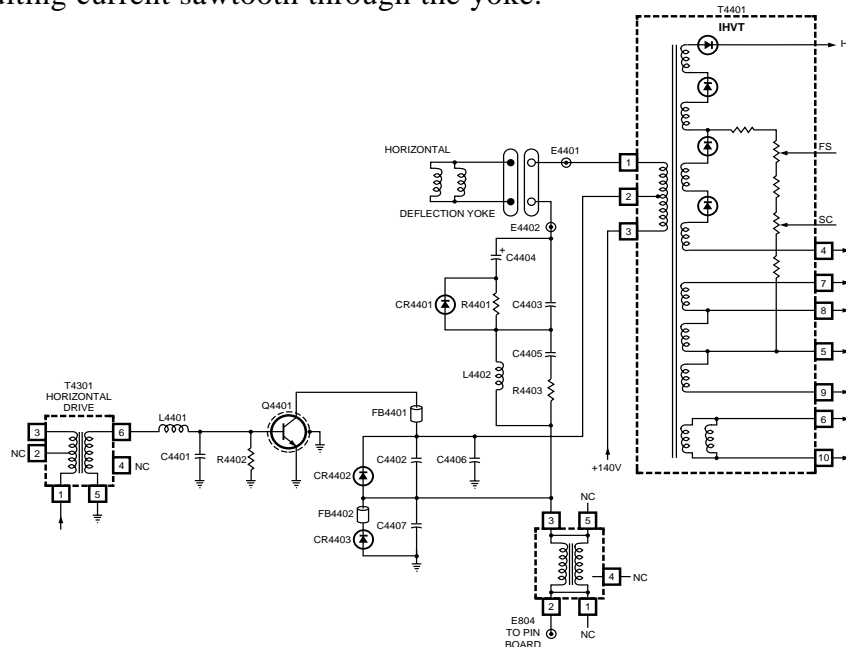
Figure 21, 27" and 31" Horizontal Output Circuit

Horizontal AFC and APC

The purpose of the AFC and APC is to maintain proper synchronization between horizontal scan and the incoming sync signal. The T-Chip employs a "two-loop" approach to accomplish this task. The first loop is the AFC and second loop is the APC. The AFC phase locks the horizontal oscillator to the incoming sync signal. The APC locks the phase of the horizontal output to the phase of the horizontal oscillator. This type of frequency control system is similar to the one used in the CTC149 and is superior to the single loop system seen in the CTC159 and CTC169 family of chassis. This system is superior because it is adjustable for good noise immunity in the presence of noisy signals and can track rapid phase changes in signals from VCR's. There is a one bit register in the T-Chip that is adjusted to obtain optimum performance. The register is called AFC Gain. This register is adjusted at the factory and cannot be aligned in the field. The external circuit at pin 23 of U1001 is the loop filter for the phase lock loop (PLL) and is used to optimize the frequency response of the AFC loop.

The APC loop is used to track out the phase errors due to variable delays in the horizontal driver and output circuit. The APC has a two bit register (APC Gain) that controls the gain of the APC loop. APC Gain like AFC Gain is pre-set at the factory and cannot be adjusted by the service technician. The reference signal for this loop is a flyback pulse applied to an RC network and input to U1001 pin 25.
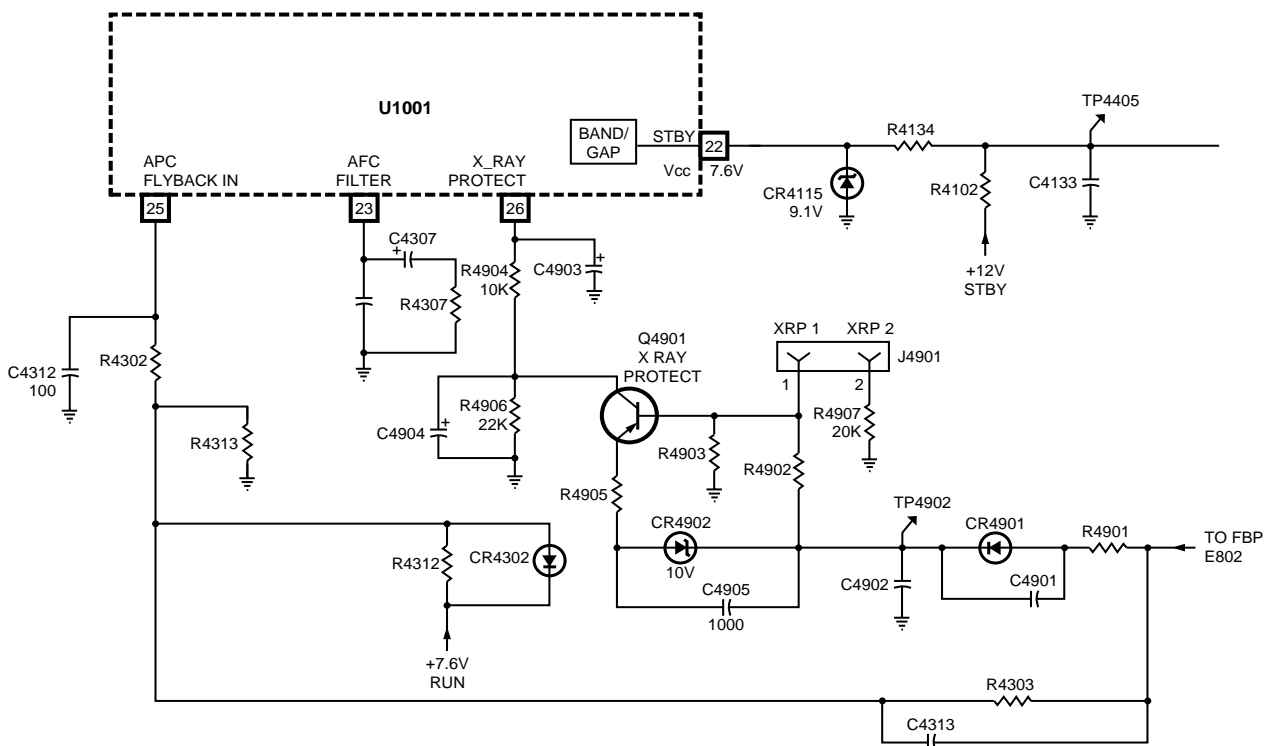
Figure 22, Horizontal APC/AFC and XRP Circuit

Although AFC and APC Gain are fixed adjustments at the factory, two horizontal alignments are accessible to the service technician:

Horizontal Alignments

- Horizontal Frequency

- Horizontal Phase

U1001 has a five bit register to adjust the free-running frequency of the horizontal oscillator. This is not unlike the coil adjustments performed on previous chassis. The oscillator is completely contained within the T-Chip with no external coils to adjust. The adjustment is made over the serial data bus via the service menu. See the section on system control in this publication or consult the service data on using the service menu.

Horizontal Frequency Adjustment
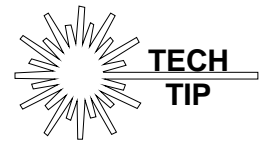
1. Set service menu to alignment #01.

2. Adjust value range for stable or slowly moving horizontal lines.

Note: Be careful not to adjust the horizontal frequency too low or the set can go into XRP shutdown. If this happens, the set will not turn back on to facilitate changing the value high to prevent shutdown.

TECH TIP

The technician can re-start the TV after an alignment induced shutdown in two ways. One step is to replace the U3201, the EEPROM, with a new IC that has the nominal values loaded. This means of course the entire chassis, including the tuner, will have to be re-aligned. The other step is to *temporarily* add additional capacitance across the retrace capacitor, C4402, to de-tune the circuit. This will lower the high voltage allowing the set to stay on while the horizontal oscillator frequency alignment is changed.

Shutdown Recovery

TECH TIP
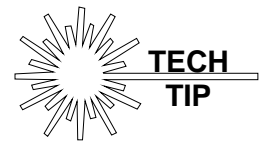
Some precautions in adding capacitance must be followed in order to prevent damage to the horizontal circuit. The 20" versions will require an extra 1000 to 1500 pf, while the 25" versions will require a bit more, approximately 3000 pf. Both of these versions have pin free yokes so double the capacitance will not be dangerous (parallel an identical C4402 across the one in the circuit - stock number 214751). The versions with diode modulator pin correction (27" and the 31") are a little trickier. These sets have a balance between the resonant frequency of the horizontal scan circuits and the EW pin output circuit. If this balance is disturbed too much, damage to one of the damper diodes can occur. This damage is always proceeded by a significant reduction in horizontal scan and usually takes a long time to occur so care can be taken to avoid problems. It is best to keep additional capacitance under 2000 pf. if possible. It may be necessary to add additional capacitance across the pin retrace capacitor, C4407, to maintain the balance. A rule of thumb is, "add four times as much capacity to C4407 as you add to the retrace cap." **Capacitors used must have a working voltage of at least 1.6 kV. Any additional capacitors must be removed once the horizontal frequency has been adjusted.**

U1001 also has a four bit register to control sync to flyback phase. This is accessible to the servicer through the service menu and is used to center the video on the CRT.

Horizontal Phase

1. Set service menu to alignment #02.

2. Adjust value range to center picture left to right.

Troubleshooting

Dead Set

A failure in the horizontal circuitry will most likely cause a dead set symptom.

1. Check the collector of Q4401 for +140 volts. If missing, check for a shorted Q4401 and troubleshoot the power supply. If present, go to the next step.
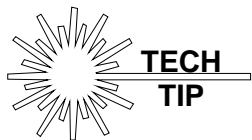
Note: On the CTC175 chassis with a series pass regulator power supply, if the horizontal output transistor is shorted, check for a 7shorted Q4150 in the power supply. It is likely a shorted horizontal output transistor will take out the regulator.

2. Check for 7.6 volts on pin 22 of U1001. If it is not there, check the 12 volt standby supply. If it is there go to the next step.

3. Check pin 24 of U1001 for horizontal drive pulses when the power button is pressed. If no pulses are seen, see dead set troubleshooting in the "System Control section of this publication. If they are present, go to the next step.

4. Check for horizontal drive pulses on the emitter of Q4302 and the collector of Q4301. If they are missing, check the corresponding stages. If they are there, go to the next step.

5. Check the drive to signal to the base of the horizontal output transistor, Q4401. If it is present, suspect a defective Q4401. If it is not, suspect a defective T4301
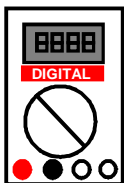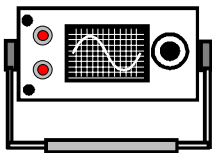
No Horizontal Sync

1. Check to see if the horizontal frequency alignment in the service menu will correct the problem. Make note of the original alignment parameter so it can be returned if aligning does not correct the problem.

2. Make sure the problem is a horizontal sync problem by comparing the horizontal drive signal to incoming video sync (one complete horizontal drive cycle begins and ends with the horizontal sync in the video).

3. Check for the APC feedback signal to pin 25 of U1001. If missing, trace it back to T4401, the IHVT. If the signal is present at pin 25, go to the next step.

4. Check the APC filter voltage on pin 23 of U1001 with service data. If it is incorrect, suspect the components off pin 23.

The electron beam scanning the face of the CRT must travel further to the corners than it does to the edges. If not corrected, the picture would have an hourglass shape called pincushion distortion. The pincushion correction circuit modulates the horizontal yoke current at a vertical rate to correct the distortion. The pincushion correction circuit is used in 27" and larger instruments. Sets with CRT's smaller than 27" use the horizontal linearity coil and a pin corrected yoke.

Pincushion Correction

U1001 produces a vertical rate parabola at pin 19 that drives the pincushion correction circuitry. This output has bus controlled DC and AC components which are aligned over the serial bus. The DC register is controlled by a four bit register, E-W DC. This is used to align raster width. The AC component is controlled by a three bit register, E-W Amplitude. This controls the amount of pin or barrel distortion in the raster.
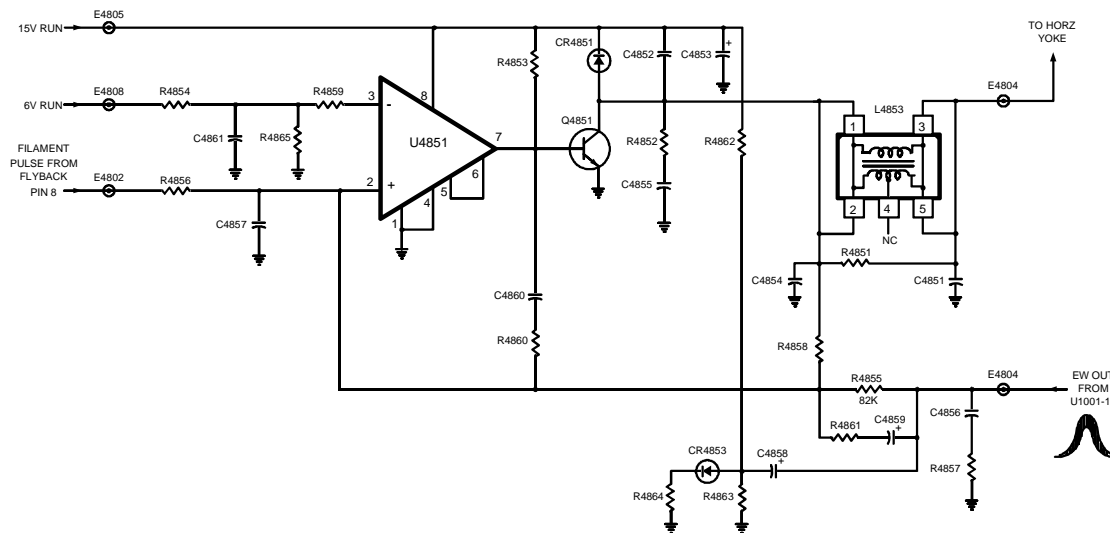
Figure 23, Pincushion Correction Circuit

The vertical parabola from pin 19 of U1001 is combined with a filament pulse at pin 2 of U4851. The DC reference for the inverting input on pin 3 of U4851 is set to approximately 3.5 volts by the divider composed of R4854 and R4865. U4851 turns on Q4851 at the horizontal rate while the amplitude of the signal is modulated at the vertical rate. C4851 is connected to the low side of the horizontal yoke . When Q4851 is on, current is pulled from the horizontal yoke, through L4853 to ground through the collector-emitter junction of Q4851. This lowers the voltage on C4851 increasing the current flow through the horizontal yoke. Increased current flow through the yoke will cause the raster to be wider. In this way, the current through the yoke is modulated to correct for pincushion distortion.

When Q4851 turns off, the energy stored in L4853 is released. This voltage is dumped to the 26 volt supply when it is high enough to forward bias CR4851 (approximately 26.6 volts). This prevents excessive voltage from damaging Q4851.

TECH TIP
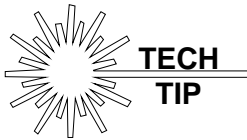
Note: Malfunctions in the pincushion circuit can make the 26 volt supply rise causing repeat failure of the vertical output IC, U4501.

Pincushion Alignments

(27" and 31" only)

Pincushion E-W DC

1. Set the service menu to alignment #03.
2. Adjust the value range for approximately 1/2 inch overscan on the left and right sides.

Pincushion E-W Amplitude

1. Set the service menu alignment #04.
2. Display a crosshatch pattern on the screen.
3. Adjust the value range for straight vertical lines on the left and right sides.

Troubleshooting
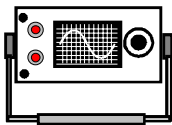
If the pincushion circuit fails completely, the picture will either go to maximum width or will pull in on the sides depending on the mode of failure. If the geometry of the picture is off due to pincushion problems, see if the alignment procedure will help correct the problem. Make sure to note the parameter setting of the adjustment so they can be returned to their original settings if it is found not to be an alignment related problem.

Width/Hourglass

1. Check for a defective Q4851.
2. Check the DC voltages on U4851.
3. Check for the E/W drive signal on E4804 and the filament pulse on E4802.

X-ray Protection

The XRP (X-ray Protection) circuit shuts the TV down before high voltage climbs high enough to pose an x-ray hazard. The circuit rectifies a flyback pulse at CR4901 and applies the voltage to the base of Q4901 through a voltage divider and to the cathode of a zener diode, CR4902. Q4901 is a PNP transistor that is off under normal operating conditions. When high voltage rises high enough to overcome the 10 volt zener diode, CR4902 conducts and applies a positive voltage to the emitter of Q4901, turning it on. This applies a positive voltage to U1001 pin 26, causing horizontal drive to shutdown. The shutdown is a latching shutdown and will reset when the voltage on pin 26 is removed; however, the system control circuit will toggle the set to the "off" state if the set fails to start after three tries. The power on/off button will have to be pressed to attempt to re-start the set again.

Troubleshooting

A failure in the XRP circuit can shut the TV down and/or keep the set from turning on completely.

XRP Shutdown

1. If the set tries to start three times and then stays off (noticeable by the degaussing relay clicking), the set is in XRP shutdown. Also, monitor pin 26 of U1001 with an oscilloscope while pressing the power button. If DC voltage appears momentarily as the set shuts down, the set is going into XRP shutdown. If no voltage appears at pin 26 and the set fails to turn on, XRP shutdown is not the problem.
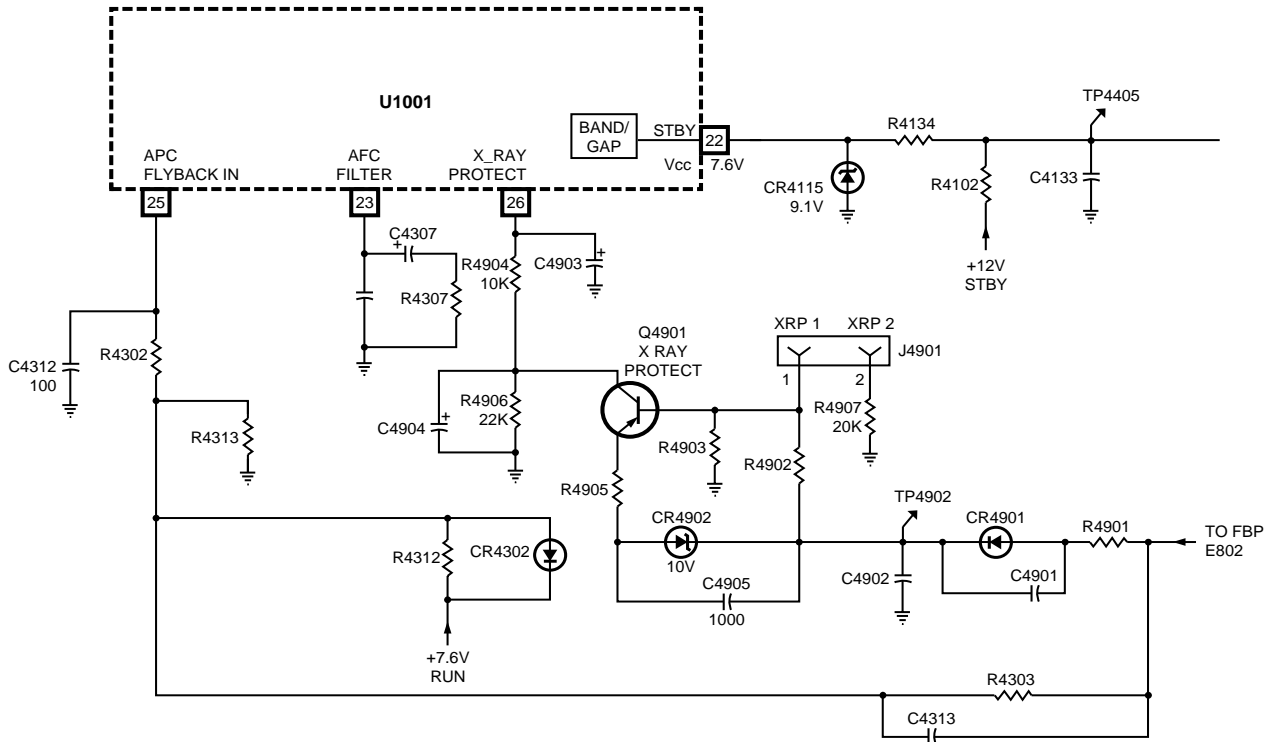
Figure 24, XRP and 7.6 Volt Regulator Circuit

2. Check Q4901 and CR4902. Note: all the components in the XRP circuit are safety critical components and must be replaced with the exact originals. Follow the guidelines set forth in the service data.

Horizontal Standby Regulator

The 7.6 volt standby supply is regulated by an internal regulator at pin 22 of U1001. The 9.1 volt zener diode, CR4115, is for protection against excessive input voltage. This supply is used by the horizontal drive circuits to start the set from the standby mode.

Troubleshooting

The television will not operate without the 7.6 volt standby voltage on pin 22 of U1001.

No 7.6 volt Standby

1. Check the 12 volt standby supply.

2. Check for a shorted CR4115.

3. Check for an internal short or a leaky pin 22 to ground (if 7.6V < 7.3V). If it is leaky or shorted, U1001 will have to be replaced and completely realigned.
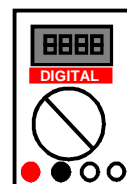
Vertical The vertical circuit in the CTC175/176/177 is very similar to the previous linear vertical circuits using a vertical output IC. One important difference to point out is this vertical circuit is DC coupled instead of capacitively AC coupled. The DC coupled circuit has advantages of fewer parts, lower cost and less dependence of linearity on electrolytic capacitor tolerance and aging. The "S" correction is accomplished inside the LA7610 T-chip, U1001.

Because of DC coupling, the DC level of the vertical reference ramp from U1001 pin 17 affects vertical centering. This provides a new adjustment, Vertical DC (vertical centering), to be included in the digital alignments. It compensates for tolerances in the reference ramp DC voltage.

The vertical circuit acts as a voltage to current converter. It converts the vertical rate DC ramp out of the T-Chip to a current ramp through the yoke to deflect the electron beam from top to bottom on the CRT. U4501 is an inverting amplifier that sinks current at pin 5 when pin 1 is high and sources current from pin 5 when pin 1 is low. U4501 is supplied by the 26 volt run source from the IHVT.
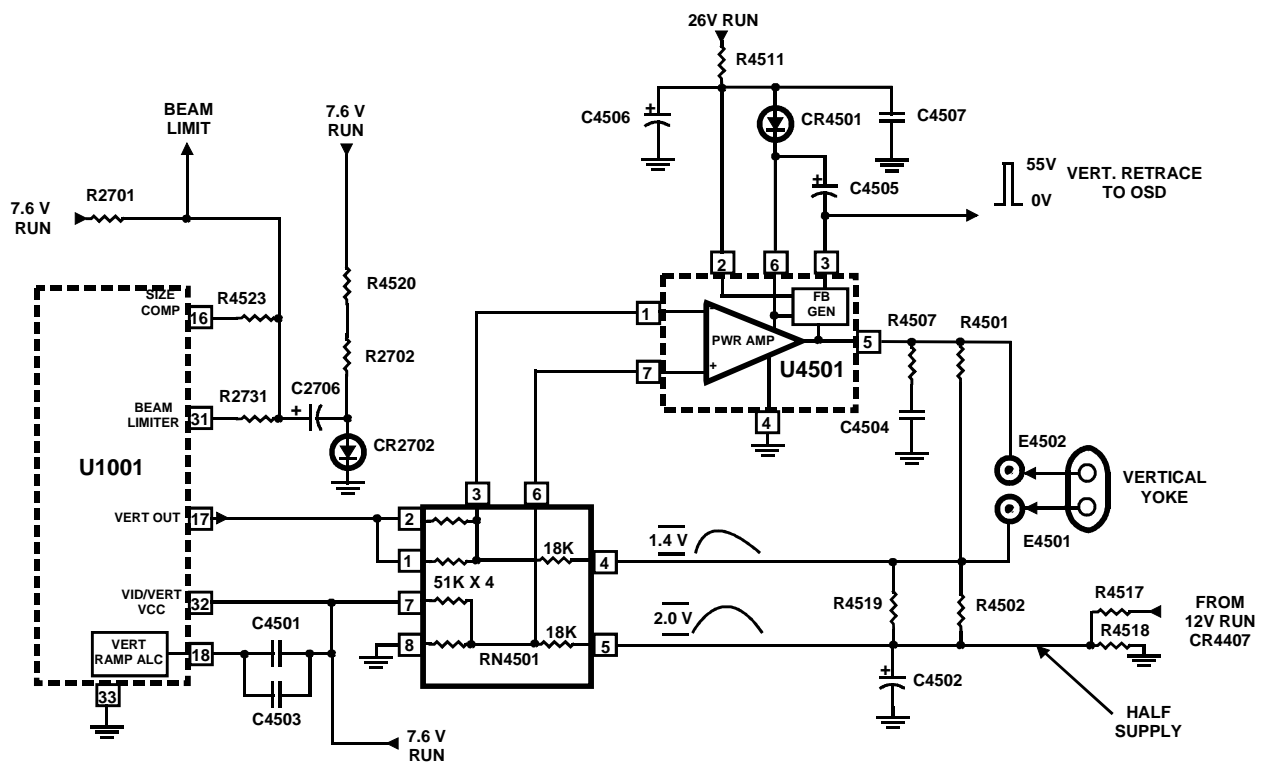
Figure 25, Vertical Deflection Circuit

The low side of the yoke connects to a "half supply" (approximately half of the 26 volt supply) developed from the 12 volt run supply. R4517 limits the current in the yoke to keep the beam from deflecting off the screen if U4501 shorts to ground or to the 26 volt source. R4518 adjusts the circuit for different screen sizes and is currently only used in the 20″ sets. C4502 is used as a filter for the 12 volt run supply and with R4518 helps reduce the vertical rate ripple current on the 12 volt run supply. R4519 and

R4502 form a current sense resistor that develops a voltage drop across it proportional to the yoke current. A fraction of this voltage from the "half supply" is input to pin 5 of RN4501 and an equal fraction of voltage is input to pin 4 of RN4501. Both signals feed back equally to the inverting and non-inverting inputs of U4501 resulting in no error output. This cancels any parabola signal resulting from vertical rate current on C4502. The quality of the canceling effect is determined by the match of the resistors in RN4501 which in this case are matched to .5 percent.

Pin 17 of U1001 provides the vertical sawtooth to pins 1 and 2 of RN4501. The average DC level of the ramp is approximately half the Vertical VCC supplied to pin 32 of U1001 (approximately 3.8 VDC). The ramp can be adjusted +/- 150mV via the Vertical DC adjustment over the data bus. The vertical ramp and the error signal riding on the 12 volt "half" supply from the current sense resistors, R4519 and R4502, are added together and input to the inverting input, pin 1, of U4501. The 7.6 volt supply is input to pin 7 of RN4501 where it is divided down to half VCC. It is then added to the error signal riding on the 12 volt half supply from the current sense resistors, output at pin 6 of RN4501 and applied to the non-inverting input, pin 7, of U4501. The average DC voltage on pin 7 is approximately 9 volts during normal operation.

When the vertical ramp is at the bottom of the slope, pin 5 of U4501 sources current from the 26 volt supply through the yoke to the 12 volt "half supply" deflecting the electron beam to the top of the screen. As the ramp climbs in voltage on pin 1, the current source from pin 5 proportionally decreases lowering the voltage across the yoke, deflecting the beam towards the center of the screen. When the voltage on pin 1 of U4501 reaches the same voltage as pin 7, pin 5 is at approximately half the 26 volt supply. Because the low side of the yoke is tied to the 12 volt "half supply," there is no current through the yoke resulting in the electron beam being at the center of the screen. As the voltage on pin 1 of U4501 rises higher than pin 7, pin 5 begins to sink current. This causes the current to flow from the 12 volt "half supply," through the yoke to pin 5. Because the current flow reverses, the beam is deflected towards the bottom of the screen. During retrace, the ramp resets causing pin 5 of U4501 to go high, deflecting the beam back up to the top of the screen. The extra current required to deflect the beam from the bottom to the top of the screen is produced by C4505.

During scan time, the negative lead of C4505 is grounded through pin 3 of U4501. The positive lead is charged to 26 volts. At retrace, the flyback generator inside U4501 connects pin 3 to pin 2 applying 26 volts to the negative side of C4505. The charge stored on C4505 plus the 26 volts on the negative terminal produce 52 volts on pin 6. The increased B+ quickly retraces the beam to the top of the screen.

Note: A failure in the pincushion circuit can cause repeat failure of U4501. See pincushion circuit for troubleshooting hints.

TECH TIP
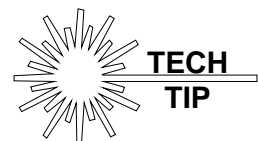
Vertical size compensation with varying beam current is achieved via pin 16 of U1001. The vertical reference ramp at U1001 pin 17 will change about 1 percent per volt change at pin 16. Pin 16 is nominally 3.8 volts (half VCC) during normal operation.

As beam current increases toward the beam limiter threshold, a point is reached when the beam sense line will begin pulling down the voltage at pin 16 through R4523. This causes about a 1.7 percent drop in the vertical reference ramp at U1001 pin 16 reducing vertical scan slightly. This prevents the picture from blooming vertically during high beam current scenes.

U1001 pin 18 is the vertical ramp ALC (automatic level control) that maintains the vertical ramp at a constant level, even if the vertical interval changes, as with a non-standard signal. C4501 and C4503 set the time constant of this amplitude regulating servo circuit. If the total capacitance were too small, vertical linearity would be affected. In extreme cases, field-to-field vertical jitter can be seen.

Troubleshooting

The vertical circuit is direct DC coupled and does not rely on capacitors for S-shaping and feedback. As a result, vertical troubleshooting can be accomplished with a digital volt meter and an oscilloscope.

TECH TIP
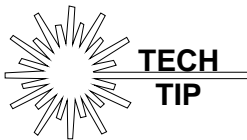
Warning: Do not try to check the DC operation of U4501 by grounding pin 1 or applying 26 volts. Damage to U4501 or any of the direct coupled stages may result.

No Vertical Deflection
1. Check for the presence of the 26 volt supply on pin 6 of U4501. If it is not present, suspect R4511 being open, possibly as the result of a shorted U4501. If it is correct, go to the next step.

2. Check for the half supply of approximately 12 volts at E4501. If it is not there, check for an open R4517. If it is there, go to the next step.

3. Check for a 2 Vpp vertical parabola on pin 1 of U4501. If it is not there, check pin 17 of U1001 for a 2 Vpp vertical ramp signal. If the ramp signal is present, suspect a defective U4501. If it is not present, go to the next step.

4. Check for 7.6 volts on pin 32 of U1001. If it is not there, trace it back to the scan derived supplies. If the voltage is correct, check pin 18 of U1001 for approximately 2.8 volts. If the voltage is wrong suspect a defective C4501, C4503 or U1001.
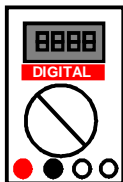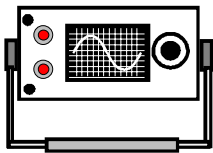
The CTC175/176/177 chassis supports a new concept in tuner design. The tuner is built on the main board instead of being a separate circuit as in the past. This change will require the technician to repair the tuner instead of replacing it. While repairing the tuner may be new for some, it is no different than working on other discrete sections of the TV. Before explaining how the new tuner works, a brief overview of how conventional tuners operate is in order.

Tuning

The CTC169 and similar television tuners use a microprocessor controlled frequency synthesizer to tune channels. The microprocessor controls a divider inside a PLL (phase lock loop) IC. This in turn produces a DC voltage that controls the frequency of the Local Oscillator. This same tuning voltage is also sent to the single tuned and double tuned circuits which are used to tune the correct band and channel frequency and match the impedance of the mixer circuit. The higher the channel tuned, the higher the tuning voltage output and the higher the frequency of the local oscillator. The local oscillator frequency is higher than the desired channel frequency so when the two signals are super heterodyned together, the difference between the two signals produces the desired IF signal. The IF filter performs the function of extracting the difference signal which produces the channel's video carrier at 45.75 MHz, the chroma carrier at 42.17MHz and the audio carrier at 41.25MHz. Changing the local oscillator frequency accordingly allows all channels to produce the same IF frequencies.

Traditional Tuners
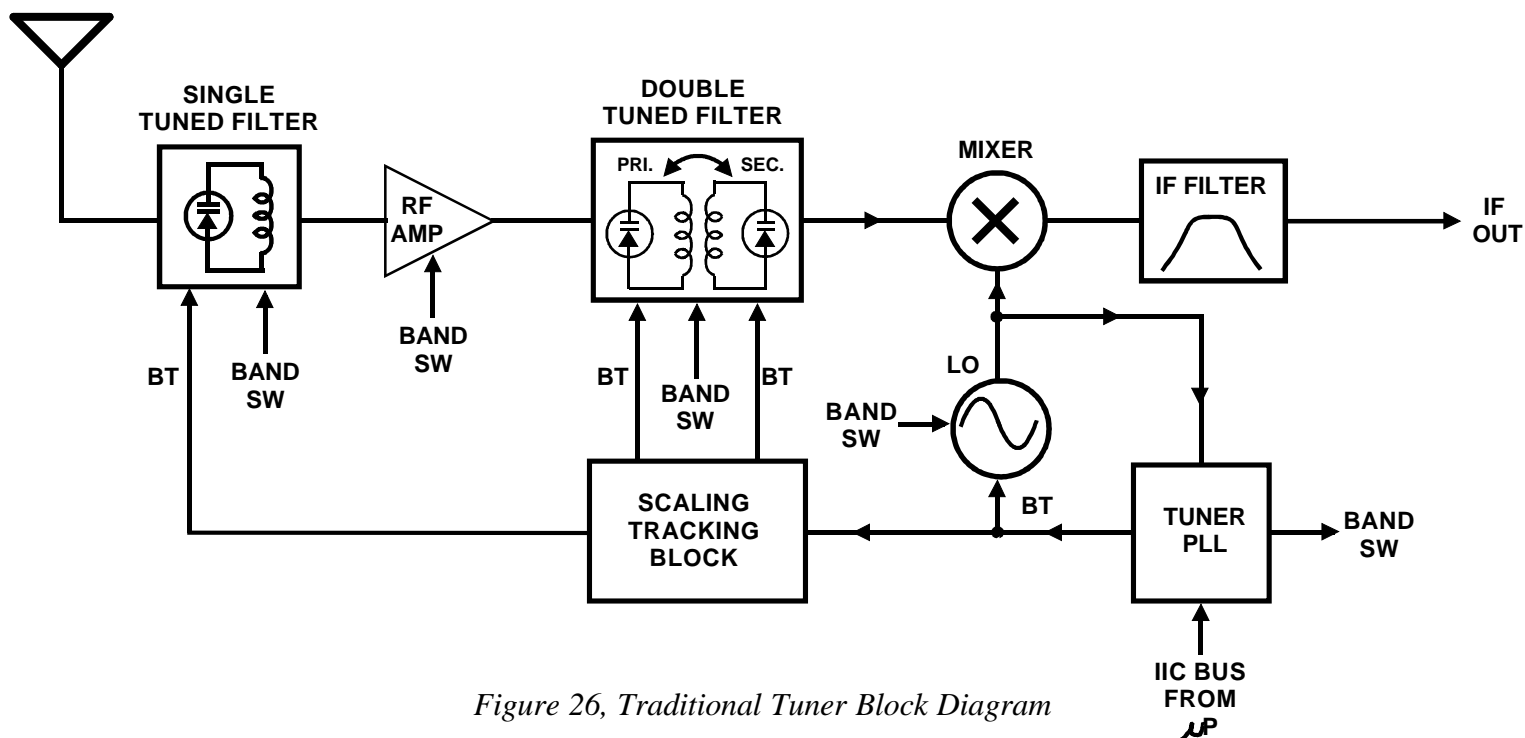
Figure 26, Traditional Tuner Block Diagram

In a traditional "track" tuner, the single tuned and double tuned circuits are all controlled by some division of the same tuning voltage. This means all stages of the tuner will proportionally "track" together as the tuning voltage changes. Because of different circuit characteristics on different channels at different frequencies, not all channels are tuned as well as others. Different stages of the tuner cannot be adjusted independently of each other because they all are controlled by some form of the same tuning voltage. This forces the design of the tuner to compromise signal performance on some channels in order to improve performance on others. The nominal performance of these tuners works well, but does not allow each channel to be optimized.

The tuning voltage to the single tuned and double tuned circuits is applied to varactor diodes. Varactor diodes are designed such that their capacitance is dependent on the voltage across the diode. As the tuning voltage varies across the diode, the varactor acts like a variable capacitor causing the tuned circuit to vary its tuning frequency. Different bands and channels are tuned in this manner. Varactor diodes are the heart of modern electronic tuners.

In addition to varactor diodes, dual gate depletion type MOS FET's (Metal Oxide Semiconductor Field Effect Transistors) are used as RF amplifiers. These transistors are very high impedance (in the mega ohms) voltage controlled devices that function very much like vacuum tubes. The N-channel depletion type MOSFET's are normally "on" without any type of gate bias. When a negative voltage is applied to the gate with respect to the source, drain current flow is reduced or pinched off entirely if the reverse bias is sufficient. Conversely, a positive voltage on the gate with respect to the source will increase drain current flow to a point. Dual gate MOS FET's have two gates both of which affect drain current. In RF amplifier configurations, the RF signal is input on Gate 1 and the AGC voltage is applied to Gate 2. As the AGC voltage rises, more drain current is produced increasing the output of the respective RF stage. As the AGC voltage decreases, the output of the RF stage decreases. These fundamental principles are important when troubleshooting.

CTC175/176/177 Tuner

The new Tuner On Board is digitally aligned. The television microprocessor adds offset voltage to the single tuned and primary and secondary of the double tuned circuits. This allows the three stages of the tuner to be independently adjusted to optimize circuit performance for each channel. This improves the tuners overall response on cable systems as well as off-air signals.

When a channel is selected, U3101 sends clock and data information to U7401 telling it what band and frequency to synthesize. The output of pins 1 and 14 of U7401 sets up the tuning voltage for the local oscillator (VT/LO) and the VREF tuning voltage (VT). The VT/LO tuning voltage adjusts the frequency of the local oscillator to produce the IF frequency of the desired channel. A sample of the local oscillators' frequency is fed back
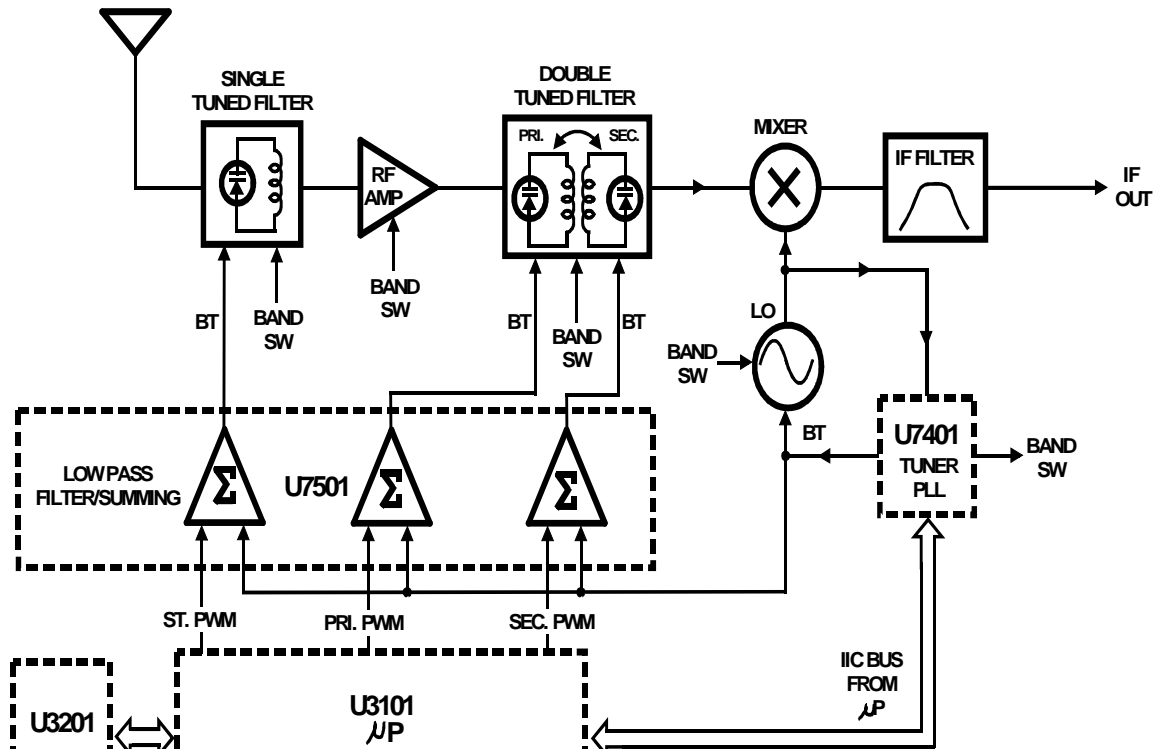
Figure 27, CTC175/76/77 Tuner Block Diagram
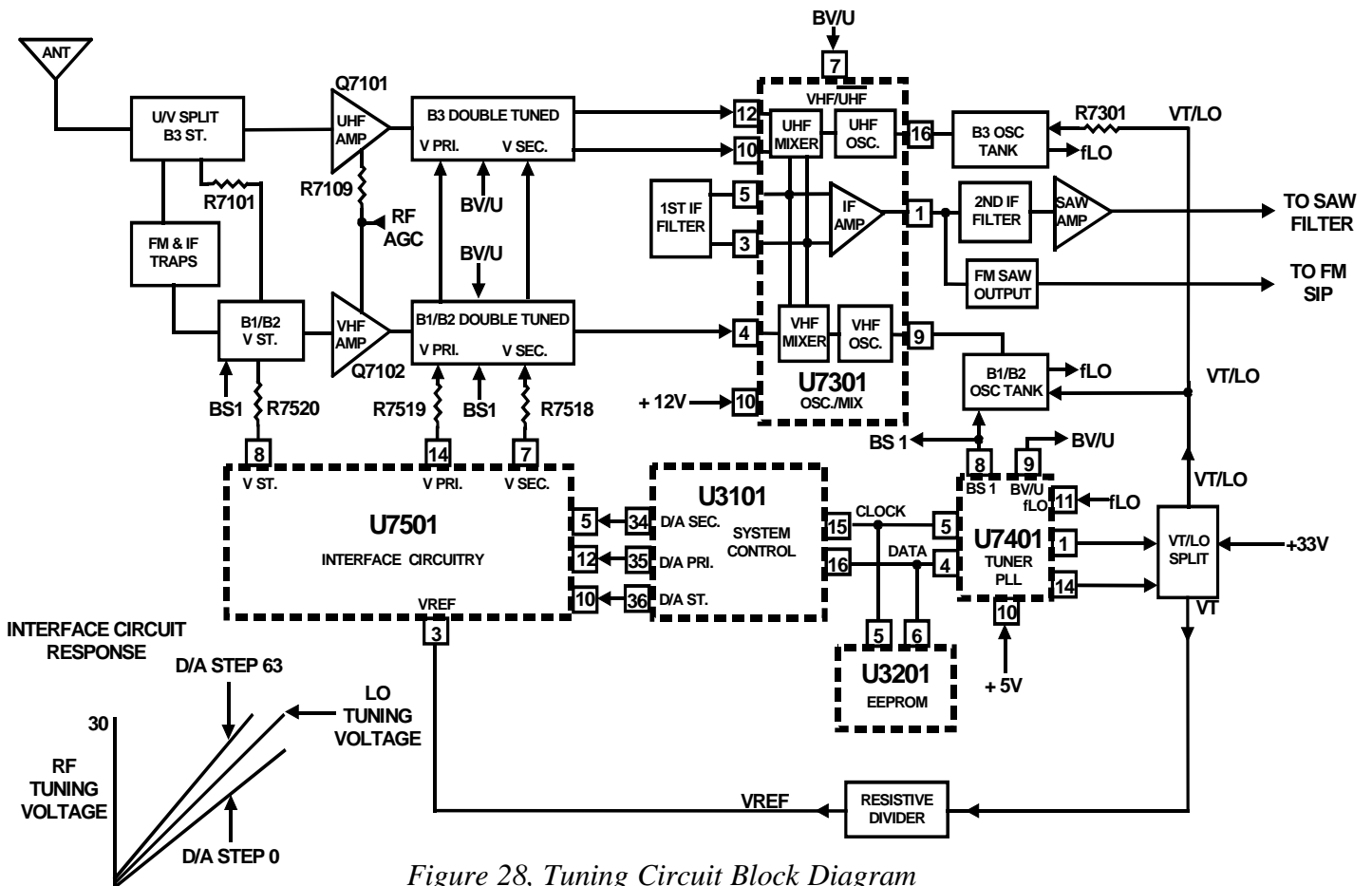
Figure 28, Tuning Circuit Block Diagram

to U7401 pin 11 to serve as feedback for the phase lock loop (digital AFT information is also fed to U3101 from U1001 over the serial bus which in turn adjusts U7401). The band switching voltages from U7401 pins 8 and 9 tell the filters what band to tune. At the same time, the VREF tuning voltage is summed with D/A voltages from U3101 and sent to the single and double tuned filters to tune the desired channel's RF carrier. The D/A levels are set via digitally stored alignment data.

The alignment data for the channels is stored in U3201, the EEPROM, and is used by U3101, the microprocessor, during channel selection. Pins 34, 35 and 36 of U3101 output a PWM (pulse width modulated) signal that is low pass filtered and summed in U7501 with the VREF (voltage reference) from the PLL circuitry. These voltages control the secondary and primary of the double and the single tuned filters respectively. The actual voltage to the filters is a function of the tuning voltage from the local oscillator plus a correction voltage from the D/A's of U3101.

U7501 forms the interface circuit that low pass filters the PWM signal from U3101 and sums it with the VREF tuning voltage. The interface circuit response is shown on figure 28. The higher the tuning voltage, the more offset voltage range from the D/A's. This is necessary because varactor diodes require more voltage across them to get the same change in capacitance at higher tuning voltages than at lower tuning voltages.

CTC175 Tuner Isolation Box

The CTC175 has a hot to cold isolation box in the input of the tuner. This is required to isolate the RF antenna connector from the AC power line potential. Capristors are used to couple the signal to the tuner as well as connect signal ground to chassis ground. The isolation box is a safety critical component and must not be bypassed.

Tuner Alignment

The tuner D/A's are aligned on 19 "data channels" that span all the frequencies to be tuned (see figure 30). Linear interpolation is used to determine the correct setting of the D/A's on channels that fall between the "data channels". This greatly reduces the number of alignments and saves space in the EEPROM. The "data channels" are aligned via the service menu described in the System Control section of this manual.
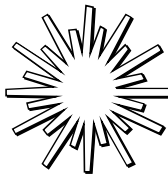
TECH TIP

There are three alignments for each data channel: Single Tuned, Double Tuned Primary and Double Tuned Secondary. Because changing the setting on one channel will affect the linear interpolation curve, all channels must be aligned if any parameter is changed. The alignment must be performed with the top and bottom tuner covers in place with the bottom shield soldered.

1. Monitor RF AGC voltage at pin 12 of the T-Chip, U1001.

2. Adjust each parameter for minimum AGC voltage on each step while attenuating the test signal appropriately.
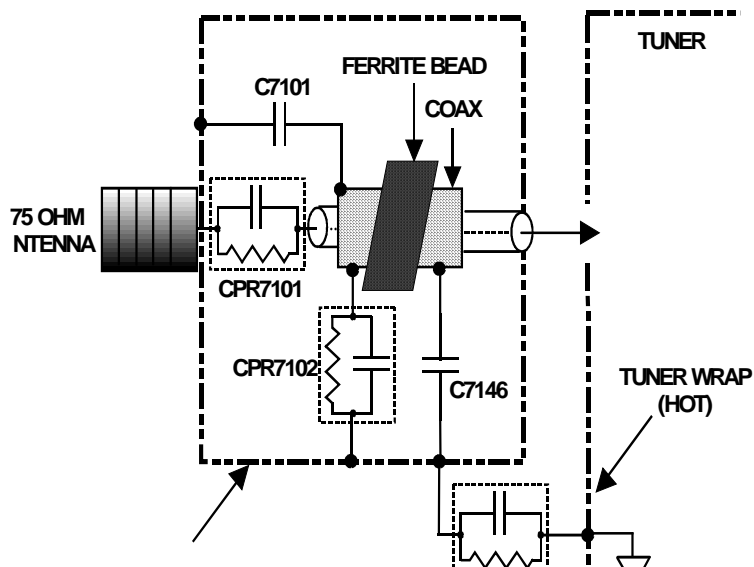
Figure 29, CTC175 Tuner Isolation Box

TEST CH.	TV CH.	BAND	PIX FREQ	MID FREQ	CHROMA FREQ	SOUND FREQ	LO FREQ
1	2	1	55.25	57	58.83	59.75	101
2	6	1	83.25	85	86.83	87.75	129
3	14	1	121.25	123	124.83	125.75	167
4	17	1	139.25	141	142.83	143.75	185
5	18	2	145.25	147	148.83	149.75	191
6	13	2	211.25	213	214.83	215.75	257
7	34	2	283.25	285	286.83	287.75	329
8	37	2	301.25	303	304.83	305.75	347
9	48	2	367.25	369	370.83	371.75	413
10	50	2	379.25	381	382.83	383.75	425
11	51	3	385.25	387	388.83	389.75	431
12	57	3	421.25	423	424.83	425.75	467
13	63	3	457.25	459	460.83	461.75	503
14	76	3	535.25	537	538.83	539.75	581
15	83	3	577.25	579	580.83	581.75	623
16	93	3	637.25	639	640.83	641.75	683
17	110	3	709.25	711	712.83	713.75	755
18	117	3	751.25	753	754.83	755.75	797
19	125	3	799.25	801	802.83	803.75	845

Figure 30, 19 Data Channels

Tuner Alignment Generator

To properly align the tuner, an RF generator capable of producing varibly attenuated, FCC frequencies up to cable channel 125 must be used. Off-air signals from an antenna or cable will not do. Because RF generators are often quite expensive, Thomson has developed an inexpensive alternative: the **TAG001.**

The TAG001 (Tuner Alignment Generator) operates off an external +5VDC supply and modulates composite audio and video signals on cables channels 2 through 125. Video IF also can be selected by entering 00. The generator is controlled by a standard RCA or GE remote control. A standard coaxial cable connects the television to the TAG001's 75 ohm "F" connector. The output level can be controlled with the built-in attenuator switches.

The TAG001 has been designed to not only be an effective tuner alignment generator, but a versatile tool for servicing all brands of television, VCR and MATV (Master Antenna Television) systems. To order a **TAG001** contact:

<div align="center">

Thomson Consumer Electronics
10003 Bunsen Way
Louisville, KY
Phone: (502) 491-8110

</div>

Tuner Alignment Generator
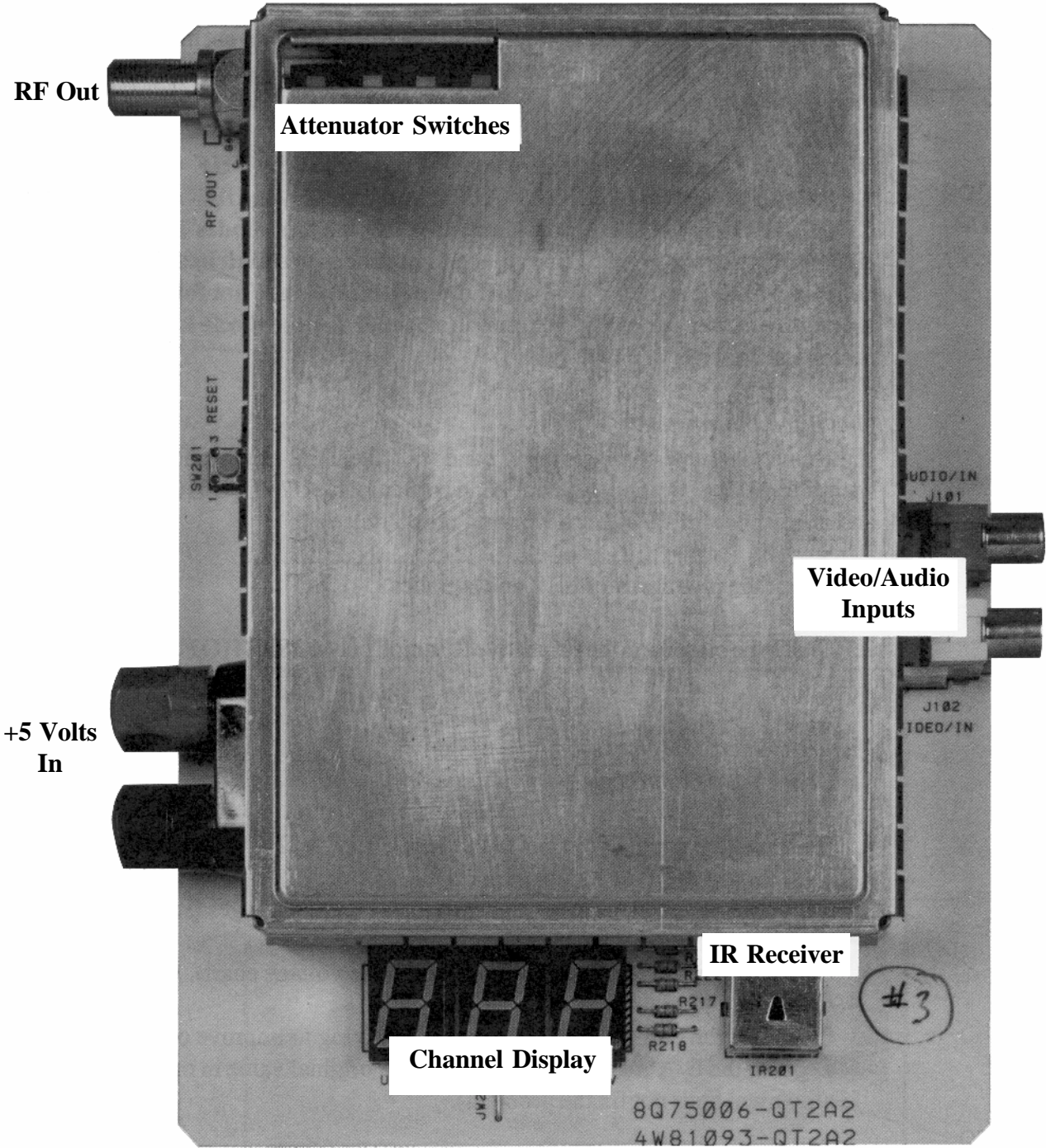
Figure 31, Tuner Alignment Generator

Troubleshooting
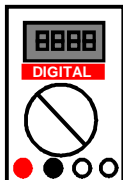
Troubleshooting the tuner is best accomplished with a digital multimeter. By making voltage and resistance checks, tuner failures can be isolated in a reasonable amount of time. Certain precautions should, however, be observed. Always put the shields back on after servicing and solder them if they were unsoldered. Make sure none of the coils in the tuner are moved or in any way repositioned (this will prevent making painstaking coil alignments later). Solder connections should be clean and smooth. Do not use more solder than is necessary.

TECH
TIP
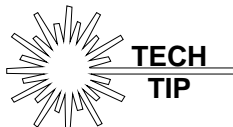
If any of the varactor diodes are replaced in either the VHF circuits (CR106, CR107, CR108, CR111, CR113 CR302 and CR305) or UHF circuits (CR101, CR102, CR103, CR114, CR301 and CR304), all the diodes in the respective circuit must be changed. The replacement diodes are matched for capacitance characteristics and come as a set. If these guidelines are not followed, the tuner will not function correctly. The stock number for the diode kit containing the matched diodes is 215494.

One Band Inoperative
If the tuner will tune channels on all bands but one, limit troubleshooting to the band specific circuitry. Obviously, if one band is functional, U7501, U3101, U3201, U7401 and at least part of U7301 are working properly.

1. Check the plus and minus 12 volt supplies.

2. Check the biasing on the respective RF amplifier MOSFET (Q7101-UHF, Q7102-VHF).

Picture Present But Not Good
1. Check the AGC voltage

2. Check all the supply voltages to the tuner: +5V, +12V, -12V and +33V.

3. Check single tuned, primary and secondary tuning voltages (see voltage chart).

4. Check for the correct voltages on U7501 (see voltage chart).

5. Check for the correct EEPROM values by trying to improve one channel by re-aligning the D/A's (make sure to record the original value in order to restore it if alignment does not fix the problem).

6. Go to number 9 on the "No Tuning" symptom below.
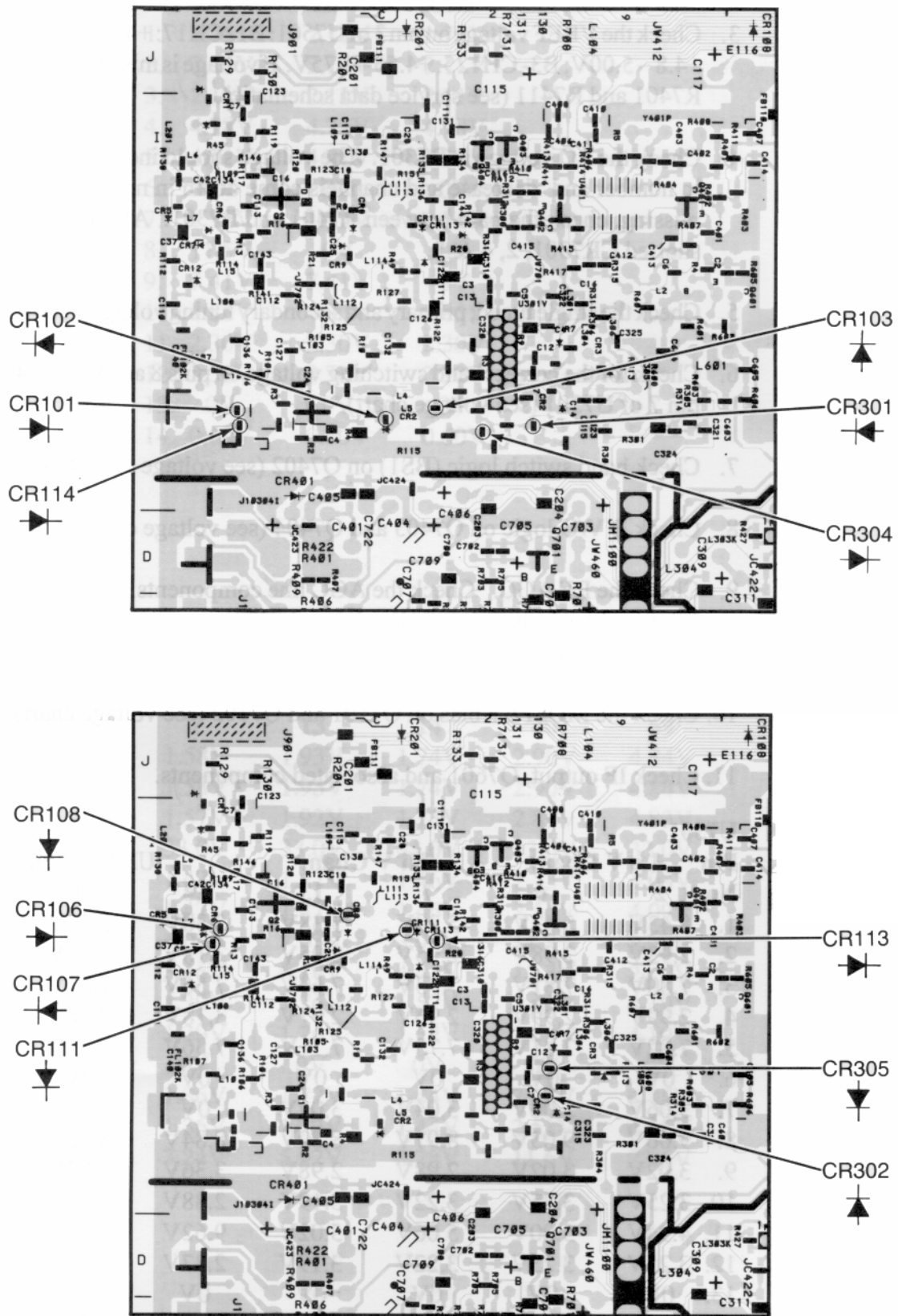
Figure 32, Varactor Diode Locations

No Tuning

1. Verify channel numbers change on the screen. If the OSD does not respond to channel change commands, the problem lies in the system control circuit and not in the tuner.
2. Check all the supply voltages to the tuner: +5V, +12V, -12V and +33V.
3. Check the VREF voltage on pin 3 of U7501: B1- CH17: +4.40 ~ 4.60V; B2- CH50: +4.8 ~ 5.00V; B3- CH125: +4.55 ~4.75V. If voltage is missing or incorrect, check R7401 and R7411 (see service data schematic).
4. Check the LO voltage at R7301. The voltage should increase as channels go up in number and decrease and channels come down in number. If the voltage is missing, check the path between R7401 and R7301. Also check for a leaky or shorted CR7301, 2, 4 & 5.
5. Check the single tuned, primary and secondary tuning voltages (see voltage chart).
6. Check for the correct band switching voltage on pins 8 and 9 of U7401 as well as pin 7 of U7301 (see voltage chart).
7. Check band switch logic (BS1) on Q7402 (see voltage chart & figure 28).
8. Check B V/U logic on Q7403 and Q7404 (see voltage chart % figure 28).
9. Check the RF AGC. Check the AGC line components: R2313, R2314, R2315, C2306 and R7130 (see service data schematic). Attenuate service modulator output. RF AGC voltage should increase.
10. Check the MOSFET bias on Q7101 and Q7102 (see voltage chart).
11. Check IF output, Q7601 and associated components.

Tuner Voltage Charts Off-Air Signal

U7301

Pin No.	Lo V Chan.		Hi V Chan.		UHF Chan.		
	2	6	7	13	14	40	69
1.	5.43V	5.42V	5.38V	5.38V	5.30V	5.22V	5.30V
2.	2.93V	2.98V	2.95V	2.95V	3.18V	3.16V	3.18V
3.	7.80V	7.81V	7.75V	7.69V	7.56V	7.51V	7.56V
4.	2.99V	2.99V	2.96V	2.97V	3.18V	3.16V	3.18V
5.	7.82V	7.81V	7.75V	7.71V	7.56V	7.51V	7.56V
6.	0V	0V	0V	0V	0V	0V	0V
7.	3.06V	3.06V	3.04V	3.01V	0V	0V	0V
8.	9.06V	9.03V	8.97V	8.89V	8.84V	8.80V	8.84V
9.	3.02V	3.02V	2.98V	2.98V	3.36V	3.33V	3.36V
10.	3.25V	3.25V	3.22V	3.19V	2.88V	2.87V	2.88V
11.	4.94V	5.00V	5.06V	5.02V	9.62V	9.58V	9.62V
12.	3.25V	3.23V	3.22V	3.19V	2.87V	2.87V	2.88V
13.	0V	0V	0V	0V	0V	0V	0V
14.	.9.05V	9.04V	8.97V	8.90V	5.43V	5.39V	5.46V
15.	3.43V	3.43V	3.40V	3.37V	2.88V	2.84V	2.88V
16.	3.44V	3.43V	3.40V	3.38V	2.89V	2.89V	2.89V

U7401

	Lo V	Hi V	UHF
1.	1.75V	2.11V	1.72V
2.	2.11V	2.11V	2.11V
3.	2.11V	2.11V	2.11V
4.	4.78V	4.78V	4.78V
5.	4.71V	4.71V	4.71V
6.	0V	0V	0V
7.	1.32V	1.32V	1.34V
8.	11.5V	0V	0V
9.	7.41V	7.41V	0V
10.	4.85V	4.85V	4.85V
11.	2.30V	2.30V	2.30V
12.	2.30V	2.30V	2.30V
13.	0V	0V	0V
14.	0.60V	0.60V	0.60V

U7501

Pin No.	Lo V 2	Hi V 6	7	13	14	UHF 40	69
1.	1.36V	1.96V	1.58V	1.93V	1.74V	2.90V	4.84V
2.	1.36V	1.96V	1.58V	1.93V	1.74V	2.90V	4.84V
3.	1.35V	1.95V	1.57V	1.92V	1.73V	2.89V	4.83V
4.	33.0V	33.0V	33.0V	33.0V	33.0V	33.0V	33.0V
5.	1.06V	1.74V	1.47V	1.87V	1.46V	2.53V	4.08V
6.	1.06V	1.74V	1.47V	1.87V	1.46V	2.54V	4.09V
7.	1.06V	6.05V	4.09V	7.03V	3.95V	11.8V	23.2V
8.	0.68V	4.57V	3.46V	6.19V	4.41V	12.3V	24.0V
9.	1.01V	1.54V	1.39V	1.76V	1.52V	2.60V	4.19V
10.	1.01V	1.54V	1.39V	1.76V	1.52V	2.60V	4.19V
11.	0V	0V	0V	0V	0V	0V	0V
12.	1.05V	1.75V	1.36V	1.72V	1.44V	2.51V	4.15V
13.	1.05V	1.75V	1.36V	1.72V	1.44V	2.51V	4.15V
14.	1.01V	6.10V	3.24V	5.92V	3.78V	11.6V	23.6V

Q7101

	Lo V	Hi V	UHF
	2	**7**	**14**
G1	0V	0V	4.84V
G2	5.03V	6.54V	7.19V
D	0.16V	0.20V	11.3V
S	0.19V	0.17V	4.83V

Q7102

	2	**7**	**14**
G1	4.64V	4.58V	4.61V
G2	5.32V	6.85V	7.19V
D	11.3V	11.2V	11.4V
S	4.08V	4.20V	11.3V

Q7401

	Lo V	Hi V	UHF
E	0V	0V	0V
B	0.60V	0.60V	0.60V
C	2.06V	3.85V	17.8V

Q7402

E	11.4V	11.2V	11.3V
B	11.3V	10.5V	10.6V
C	14.9V	11.1V	11.2V

Q7403

E	0V	0V	0V
B	0.70V	0.70V	0V
C	0.10V	0.10V	11.3V

Q7404

E	11.4V	11.2V	11.3V
B	11.0V	10.9V	10.6V
C	0.11V	0.11V	11.3V

**Tuner
Voltage Charts
Cable Signal**

U7301

Pin No.	Band 1				Band 2		Band 3
	2	**17**	**18**	**50**	**51**	**75**	**99**
1.	5.44V	5.40V	5.41V	5.40V	5.30V	5.28V	5.48V
2.	2.99V	2.96V	2.96V	2.96V	3.18V	3.17V	3.00V
3.	7.80V	7.78V	7.77V	7.75V	7.57V	7.57V	7.89V
4.	2.99V	2.96V	2.96V	2.96V	3.18V	3.17V	3.00V
5.	7.82V	7.78V	7.77V	7.77V	7.57V	7.57V	7.89V
6.	0V	0V	0V	0V	0V	0V	0V
7.	3.06V	3.04V	3.05V	3.05V	0V	0V	3.08V
8.	9.02V	9.01V	8.98V	9 00V	8.84V	8.83V	9.14V
9.	3.01V	3.01V	2.98V	2.98V	3.36V	3.35V	3.01V
10.	3.26V	3.23V	3.22V	3.23V	2.88V	2.88V	3.28V
11.	4.96V	5.04V	5.07V	5.16V	9.62V	9.60V	5.14V
12.	3.26V	3.23V	3.22V	3.23V	2.88V	2.87V	3.28V
13.	0V	0V	0V	0V	0V	0V	0V
14.	9.05V	9.00V	8.98V	9.00V	5.43V	5.42V	9.13V
15.	3.43V	3.41V	3.42V	3.41V	2.88V	2.87V	3.46V
16.	3.41V	3.41V	3.41V	3.41V	2.87V	2.89V	3.47V

U7401

Pin No.	Band 1 2	Band 2 18	Band 3 51
1.	1.74V	1.74V	1.74V
2.	2.11V	2.11V	2.11V
3.	2.11V	2.11V	2.11V
4.	4.78V	4.78V	4.78V
5.	4.71V	4.71V	4.71V
6.	0V	0V	0V
7.	NC	NC	NC
8.	11.5V	0V	0V
9.	7.47V	7.42V	0V
10.	4.85V	4.85V	4.85V
11.	2.31V	2.31V	2.31V
12.	2.31V	2.31V	2.31V
13.	0V	0V	0V
14.	0.60V	0.60V	0.60V

U7501

Pin No.	Band 1 2	17	Band 2 18	50	51	Band 3 75	99
1.	1.36V	4.63V	1.30V	5.52V	1.20V	2.21V	2.86V
2.	1.36V	4.63V	1.30V	5.52V	1.20V	2.21V	2.86V
3.	1.36V	4.63V	1.30V	5.52V	1.20V	2.21V	2.86V
4.	33.0V	33.0V	33.0V	33.0V	33.0V	33.0V	33.0V
5.	1.06V	3.62V	1.16V	4.68V	0.99V	1.90V	2.54V
6.	1.06V	3.62V	1.16V	4.68V	0.99V	1.90V	2.54V
7.	1.07V	19.8V	1.78V	27.6V	0.54V	7.20V	11.9V
8.	0.69V	24.2V	1.30V	25.3V	0.86V	7.63V	12.5V
9.	1.01V	4.22V	1.10V	4.38V	1.01V	1.96V	2.62V
10.	1.01V	4.22V	1.09V	4.38V	1.04V	1.96V	2.62V
11.	0V	0V	0V	0V	0V	0V	0V
12.	1.06V	4.36V	1.07V	4.76V	0.99V	1.86V	2.66V
13.	1.06V	4.36V	1.07V	4.76V	0.99V	1.86V	2.66V
14.	1.02V	25.2V	1.12V	28.1V	0.54V	6.91V	12.7V

Q7101

	Band 1	Band 2	Band 3
	2	**17**	**51**
G1	0V	0V	4.82V
G2	5.05V	4.17V	7.19V
D	0V	0.10V	11.3V
S	0.10V	0.10V	4.83V

Q7102

G1	4.59V	4.65V	4.61V
G2	5.44V	4.50V	7.20V
D	11.3V	11.2V	11.1V
S	4.08V	3.71V	11.0V

Q7401

E	0V	0V	0V
B	0.60V	0.60V	0.60V
C	2.05V	1.65V	1.00V

Q7402

E	11.3V	11.4V	11.4V
B	11.4V	10.6V	10.6V
C	14.5V	11.2V	11.2V

Q7403

E	0V	0V	0V
B	0.71V	0.71V	0V
C	0.11V	0.11V	11.3V

Q7404

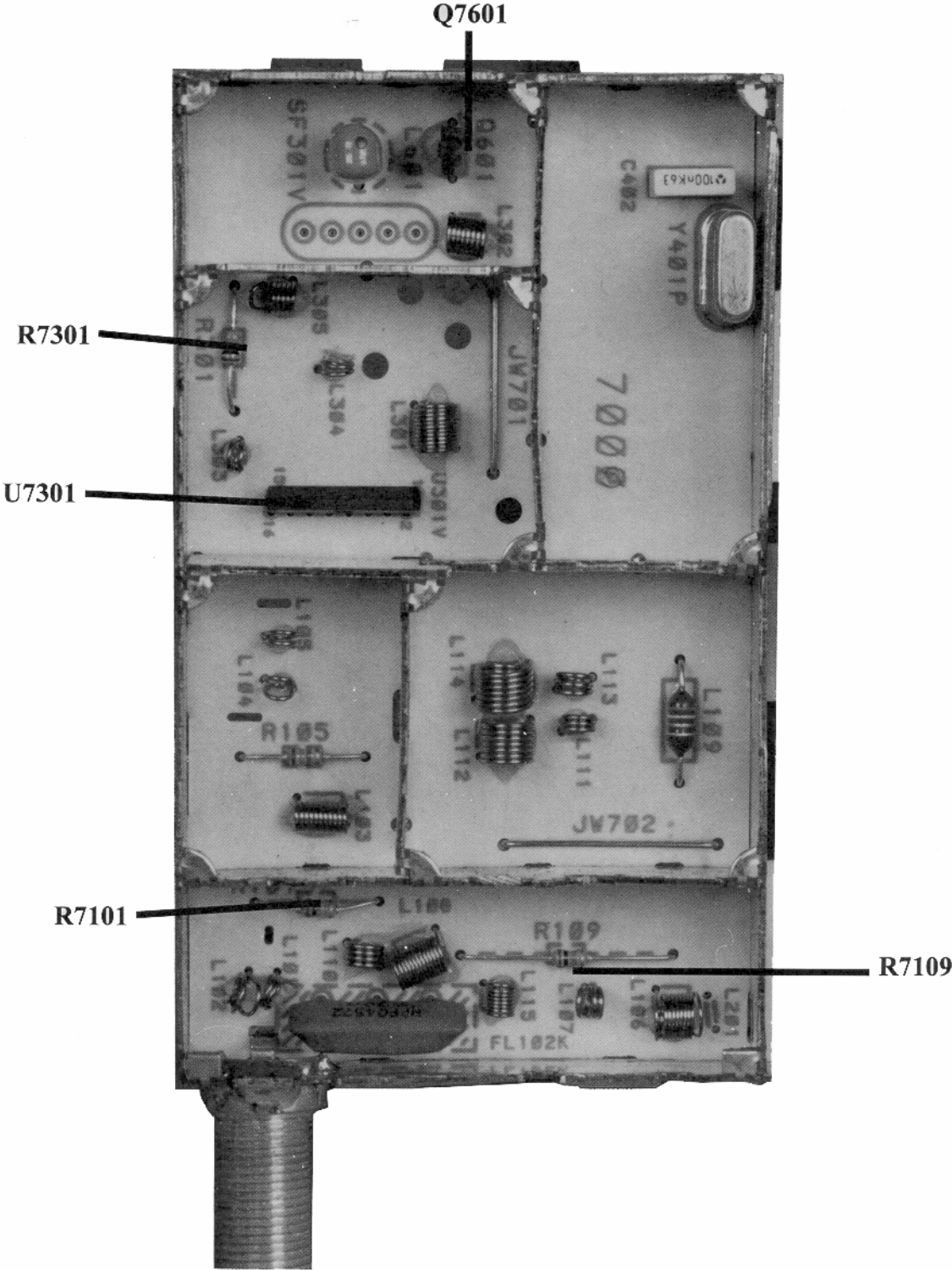| E	11.4V	11.4V	11.4V
B	11.0V	11.0V	10.7V
C	0.11V	0.11V	11.3V

Figure 3, Tuner, (Bottom View)

Figure 34, Tuner (Top View)

Video / Audio IF

The functionality of the video and audio IF circuits in the CTC175/176/177 is identical to that of previous chassis designs. New advancements in U1001 (T-Chip) make the circuits easier to service. The 45.75 MHz picture IF signal from the tuner is input to the saw filter SF2301 and coupled to U1001 pins 10 and 11. Baseband video is detected and sent to pin 51 and 63 after passing through a noise inverter. Since the video switching takes place inside U1001, pin 51 can output Aux video or TV video depending on operator selection.

AFT operation is accomplished by a 12 bit frequency counter that sends data to U3101 over the serial data bus. Because it is an actual frequency counter, there is no need for an AFT alignment coil. A sample of the detected video signals controls both RF and IF AGC. RF AGC is adjustable over the serial bus like the other alignments. Pin 12 of U1001 will sink current or let the pull-up supply source current out to the tuner. The voltage increases to increase the gain of the tuner and decreases to reduce the gain of the tuner. The RF AGC is set at the factory to get 1dB of RF gain reduction on channel 6 with 1 mVrms signal applied to the tuner input. If the RF AGC needs to be adjusted in the field, use the weakest and strongest local channels in each of the adjustment bands to minimize noise and distortion. There are four AGC alignment parameters: Channel 6, Band 1, Band 2 and Band three. These are adjusted as parameters 19 through 22 respectively (see the alignment chart in the system control section).
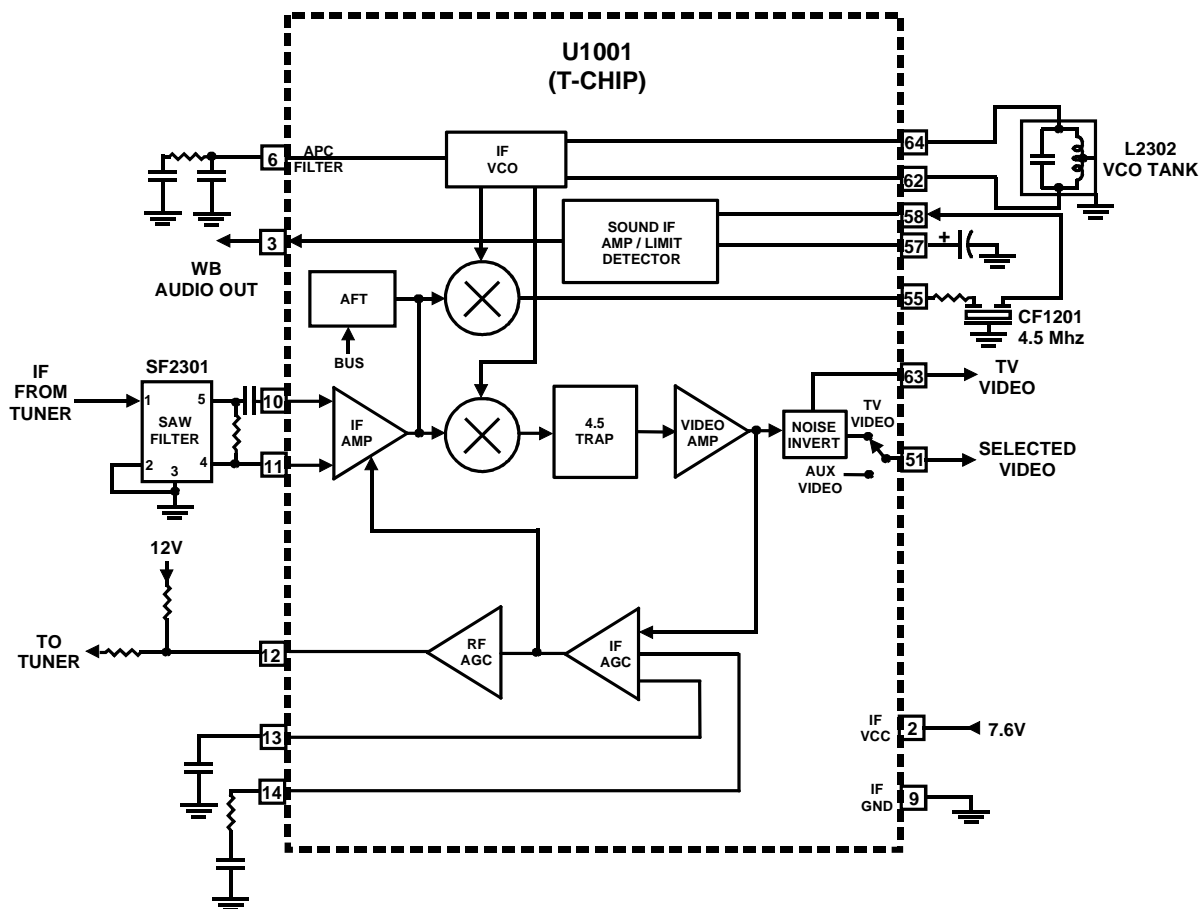

Figure 35, Video / Audio IF Circuit

The 41.25 MHz audio carrier is down converted and output at U1001 pin 55. The signals are band passed filtered by CF1201, a ceramic 4.5 MHz band pass filter and sent to an amp/limiter and mixed with the 3.58 MHz oscillator from the chroma circuit to down convert the signal a second time. The signal is then again band passed filtered, limited and finally detected. The detected wide band audio is output at pin 3 and AC coupled to the stereo decoder IC in stereo sets, and AC coupled to pin 5 in mono sets.

IF Alignments

External Marker Generator-Capable of furnishing 41.25 MHz, 45.75 MHz & 41.35 MHz, 45.75 MHz & 42.75 MHz, 4.5 MHz with AF FM.

NOTE: All alignments are bus controlled. They are accessible only through entry of the correct code. See the parameter # and value range adjustment chart in the system control section.

PLL Tuning (IF VCO Free Run)
1. Enter parameter # 14 (see chart).

2. Ground IF AGC TP2305 (pin 14 of U1001).

TECH TIP

3. Apply 41.25 MHz marker (60 mV output) to IF input (pin 1 of SF2301).

4. Connect oscilloscope to TP1201 (pin 55 of U1001). Set scope for 50ns per division.

5. Adjust parameter reading to provide a 220ns sine wave response.
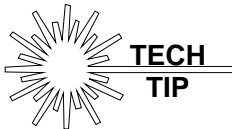
NOTE: If a 220ns sine wave response cannot be adjusted, set parameter reading to approximate mid range and adjust L2302 for a 2.2uS response.

Note: L2302 is preset at the time of manufacture and should require no further adjustment unless a 2.2uS response cannot be achieved during the parameter adjustment.

4.5 MHz Trap
1. Enter parameter # 15.

2. Make sure IF AGC TP2305 (pin 14 of U1001) is disconnected from ground.

3. Short IF AGC TP7102 (tuner side of R2313) to ground.
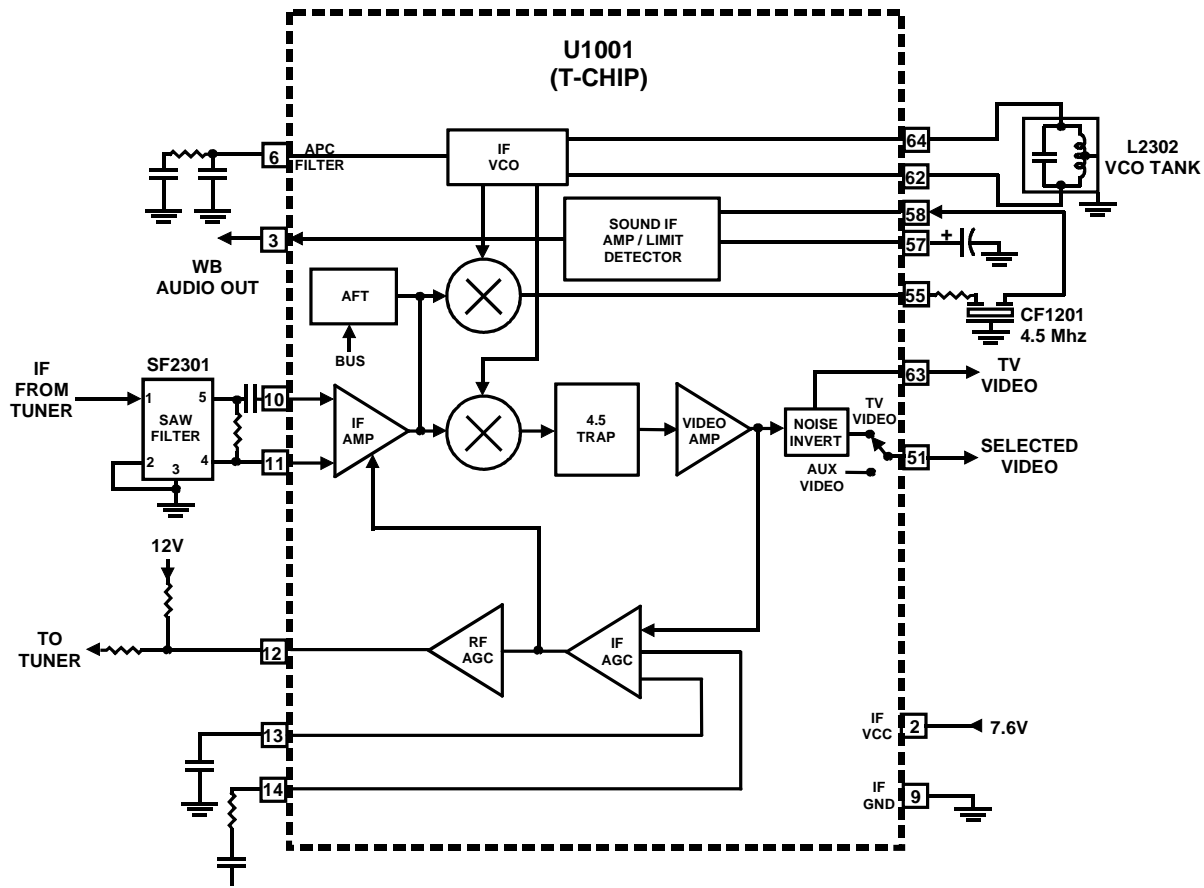
Figure 36, Video / Audio IF (repeated)

4. Apply 45.75 MHz (300mV output) and 42.75 MHz (100mV output).

5. Set parameter # 15 value to 7 (maximum).

6. Connect oscilloscope to TP2302 (pin 63 of U1001).

7. Adjust vertical scale so 4.5 MHz amplitude is 10 divisions.

8. Change 42.75 MHz signal generator to 41.35 MHz (same amplitude).

9. Decrease parameter #15 value until the 4.5 MHz signal amplitude is less than 1
   division.

Video Level
1. Enter parameter # 16.

2. Connect color bar generator to antenna input (87.5% modulation) set for super
   pulse display.

3. Connect oscilloscope to TP2302 (pin 63 of U1001).

4. Adjust value range to produce 2.0 volt p-p (sync to white) response.

FM Level (Wideband Audio)

1. Enter parameter # 17.

2. Connect signal generator to sound output TP1201 (pin 55 of U1001) with 4.5 MHz carrier, 1 KHz modulation, with 25 KHz deviation.

3. Connect IF AGC TP2305 to ground.

4. Connect oscilloscope to TP1202 (WBA output pin 3 U1001).

5. Adjust value range for 1.2 volt p-p indication of the 1KHz signal.

RF AGC

The RF AGC has been preset at the time of manufacture for optimum operation over a wide range of RF signal input conditions. Readjustment should not be required unless the tuner has been repaired, IC 1001 has been replaced, IC 3101 has been replaced, IC 3201 has been replaced, or unusual signal conditions exist such as:

1. Cable TV adjacent channel interference.

2. Picture bending and/or channel 6 color beats that are usually due to excessive RF signal input. This occurs when the receiver location is too close to the transmitting tower. It also may occur when the receiver is connected to an antenna distribution system where the RF signal has been amplified. The signal should be attenuated at the antenna input to a more satisfactory level.

3. Picture Noise caused by "broadcast noise" or weak signal. If the broadcast is "clean" and the received signal is at least 1 mV, the picture will be noise free in any area.

NOTE: Adjustment of the RF AGC parameters may not have any visible effect except under unusual conditions. Adjusting the RF AGC to one extreme of its parameter limits will usually provide a relatively poor signal-to-noise ratio, while adjustment to the other extreme of its parameter limits will cause overload conditions such as channel 6 color beats or Cable TV adjacent channel interference. If the RF AGC parameter setting is adjusted, check all local channels for proper operation. Use both weakest and strongest local signal to adjust RF AGC parameter setting.

The selected video output from pin 51 of U1001 is separated into its luma and chroma components. The luminance is input at U1001 pin 48. Pin 45 is the S-Video luminance input on sets that have an S-Video input jack. The luminance is then processed by a black stretch circuit. The DC voltage at pin 43 can put the IC in an RGB mode of operation by turning off the luminance path. The DC voltage on pin 43 must be above 1.2 volts to enable luminance. The signal is then applied to the Internal/External switch which selects between OSD and video. R-Y and B-Y from the chroma circuitry are also applied to this switch.

OSD from the system control circuitry is applied to pins 40, 41 and 42. These are the red, green and blue OSD inputs; however, on sets that do not support closed caption, only the green and blue inputs are used to produce a cyan OSD. On sets equipped with closed caption, all three inputs are used. The fast switch input controls whether OSD or video is switched out: HI = External Video (OSD) or LOW = Internal Video.

The output of the Internal/External switch produces Y, R-Y and B-Y. The three signals are sent through their respective contrast and clamp controls. These stages are controlled over the serial bus. The luminance is sent to the brightness control while the component chroma signals are matrixed and then summed with the luminance. The summed red, green and blue signals are amplified and output at pins 36, 37 and 38. The kine bias and drive controls inside U1001 are controlled via the alignment menu over the serial bus.
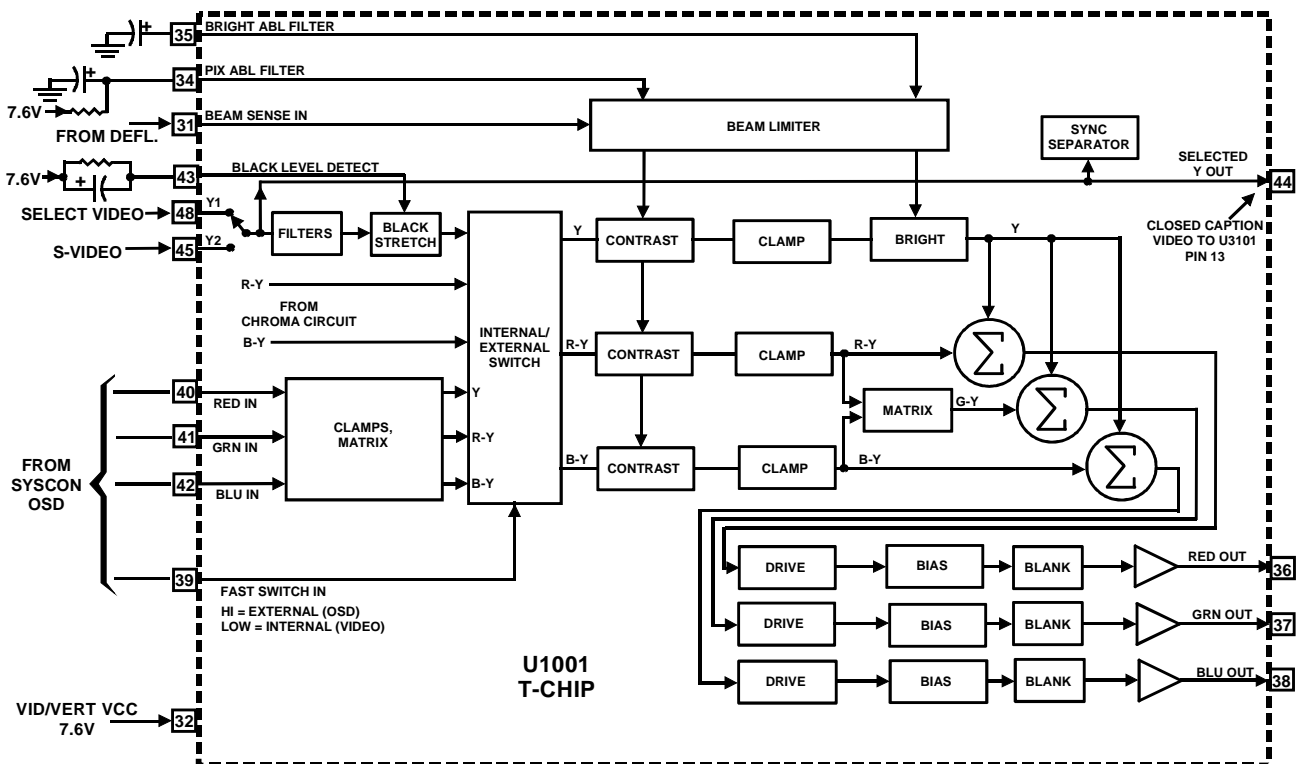
Luminance Processing

Figure 37, Luminance Processing

The beam sense input is at pin 31 and is used to reduce brightness and contrast during high beam current scenes to keep the CRT from "doming." The circuit is active below 6.2 volts.

The selected Y out at pin 44 is used as the video source for the closed caption decoder inside U3101. This signal is not used on sets that do not support closed caption. Power for the luminance processing circuits inside U1001 is derived from the 7.6 volt supply on pin 32.

Troubleshooting

No Luminance
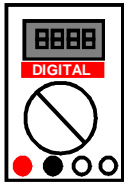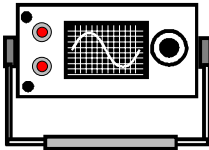
1. Check the brightness and contrast controls from the user menu. If the menu is not visible, push "reset" on the remote.

2. Check the input signal at Y1 and Y2. It should be approximately 1Vpp.

3. Check for the signal at the selected Y output on pin 44. It should be the same as Y1 and Y2.

4. Check the beam limiter control voltage at pin 31. The circuit is active below 6.2 volts.

5. Check the Fast Switch input at pin 39. A voltage equal to or greater than 1.7 volts will blank the video to let OSD through.

6. Check the RGB mode switching on pin 43 of U1001. Luminance is enabled above 1.2 VDC.

Figure 38, Chrominance Processing

Chrominance Processing

Chroma processing in U1001 is performed in much the same fashion as in the past. Pins 49 and 46 are the two chroma inputs to the 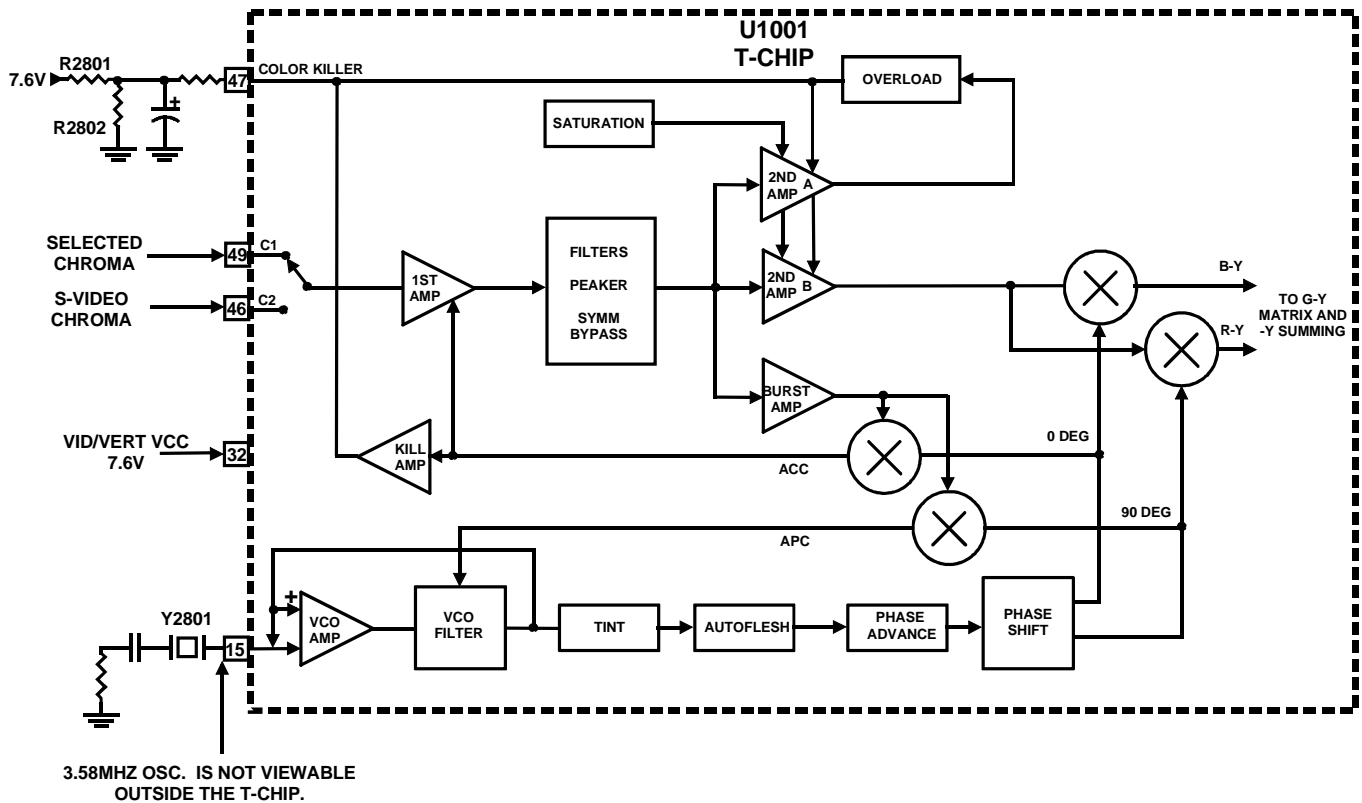IC. Pin 49 is selected chroma that can be either from an Aux video source or TV video. Pin 46 is S-Video chroma from the S-Video jack on sets that support S-Video. The incoming chroma is applied to a filter block. There are two filters in this block. The peaker is used to peak up the chroma to compensate for the high end roll-off of the IF circuit. This filter is turned on for TV video. The symmetrical filter bandpasses the chroma and is used for Aux and S-Video chroma. The bypass mode is not used in the CTC177 chassis family. The chroma is then sent to the 2nd chroma amp stages. Here, color saturation is controlled by the serial bus. The chroma signal is mixed with the 0 and 90 degree phase shifted 3.58 MHz to demodulate R-Y and B-Y. The burst signal is used in the ACC and APC circuits to control color phase and color killer circuit. Pin 47 is 3.8 volts or greater with a color signal present and low when burst is not detected. The color killer can be defeated by applying 3.8 volts DC to pin 47.

The biggest difference with the chroma circuit is the 3.58 MHz oscillator at pin 15 of U1001. The crystal is in series with the comparator circuit. When the oscillator is locked on frequency, no oscillator voltage is present on pin 15. This means the 3.58 MHz oscillator cannot be viewed outside the IC with an oscilloscope as in the past. The oscillator is used to recreate the chroma carrier to demodulate the R-Y, G-Y and B-Y. The tint and auto flesh controls affect the phase of this signal to correct fleshtones. The signal is then shifted 90 degrees and sent to the R-Y demodulator while the 0 degree signal is sent to the B-Y demodulator.

The output of the chroma circuit is sent to the Internal/External switch where it is switched with the OSD (see luminance circuit) and matrixed to demodulate G-Y.

Troubleshooting

Color problems can best be diagnosed using an oscilloscope and a digital voltmeter.

No Chroma

1. Check the Color and Tint controls from the user menu.

2. Check the chroma input level at U1001 pins 49 and 46. It should be approximately 300 mVpp.

3. Defeat the Color Killer circuit by applying approximately 4 volts DC to pin 47 of U1001. Free running chroma should be viewable on the screen (barber pole) if the 3.58 MHz oscillator is running.

Autocolor / Autoflesh Confirmation

Turn Auto color on and off from the video menu while viewing an NTSC color bar signal.

TECH TIP
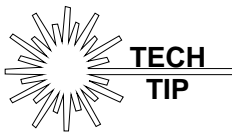
• Magenta bar should shift towards red.

• Chroma saturation should reduce slightly.

Note: The value of R2801 and 2802 is very critical for proper color saturation.
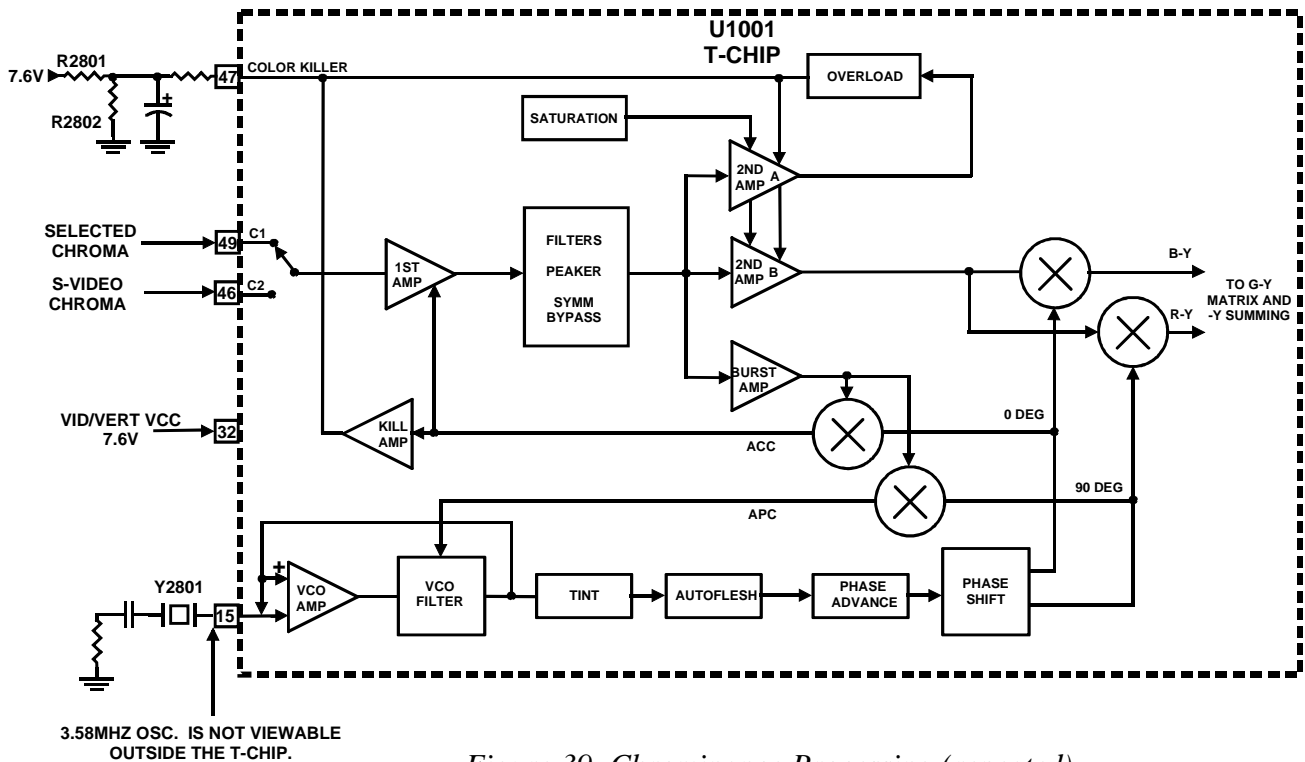
Figure 39, Chrominance Processing (repeated)

The audio circuits of the CTC177 chassis family are of two types: Mono and Stereo. In the Mono sets, wide band audio from the IF circuit is output at pin 3 of U1001 and coupled back into pin 5. The right channel of the audio circuitry serves as the mono channel. The audio signal is output at pin 59 and sent to the discrete push-pull audio amplifier and out to the speakers. Mono sets do not support audio In/Out jacks.

Audio Processing

The Stereo TV's audio is selectable in U1001 from the Aux inputs (if supported by the model) or from the stereo decoder IC, U1701. Left and right audio from the audio jacks are input to U1001 pins 7 and 8. All audio selection and volume controlling take place inside U1001. There are no external switching IC's. Wideband audio from the IF circuit is output from U1001 pin 3 as in the mono sets; however, the signal is sent to pin 5 of the stereo decoder, U1701. U1701 decodes the stereo information and outputs left and right information on pins 14 and 13. These are sent back to U1001 pins 4 and 5 where they can be selected. The selected audio is output on pins 60 and 59 where it is buffered and sent to the left and right hi-fi audio output jacks. It also goes to the television's internal stereo amplifier, U1901 and out to the TV's speakers.

U1701 informs U3101, the system control microprocessor, of the presence of a stereo broadcast with a LO out of pin 20. U3101 can then select Stereo or Mono with a LO or HI from pin 23.
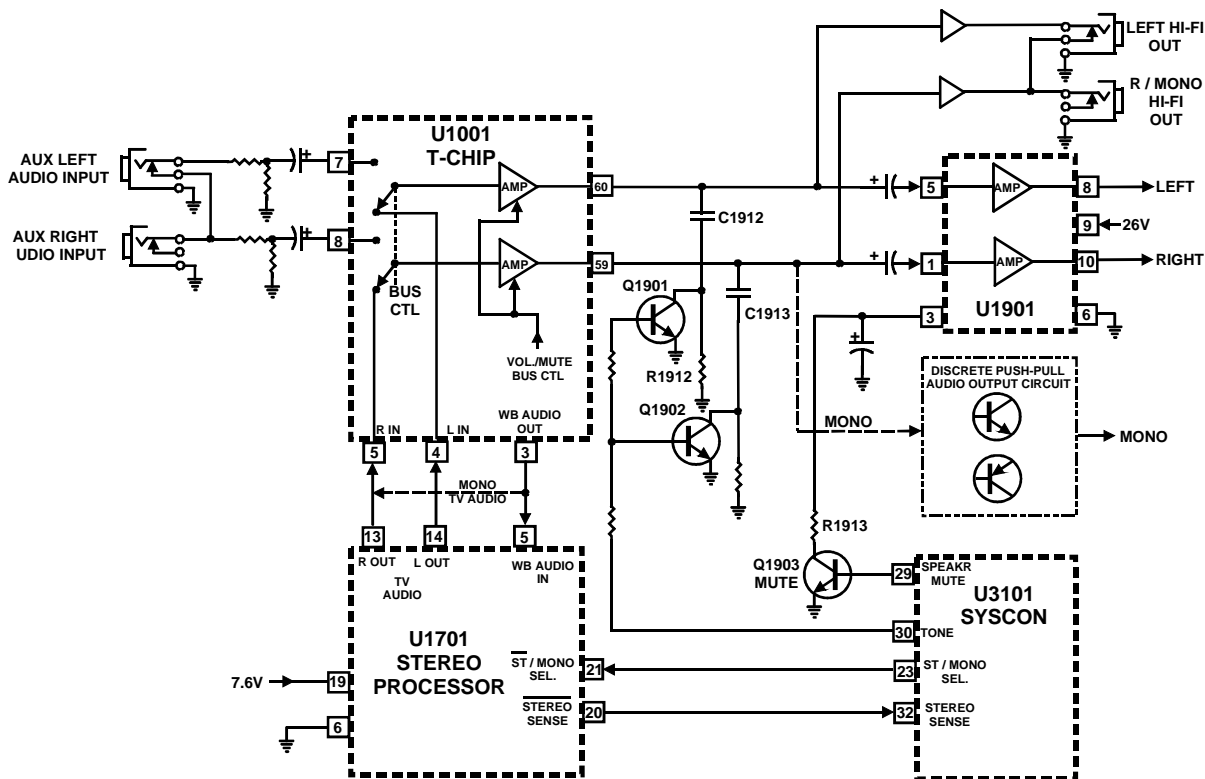

Figure 40, Audio Processing

Pin 29 of U3101 outputs a HI to Q1903 which pulls pin 3 of U1901 LO to mute the speakers during power on and when the speakers are turned off via the Audio menu. The normal Mute function on the remote control is controlled inside U1001 via the data bus. The Tone can be set to either High with a LO out of pin 30, or Low with a HI out of pin 30. In the High mode, Q1901 and Q1902 are off leaving R1912 and R1913 in series with C1912 and C1913. When Low Tone is selected, Q1901 and Q1902 turn on coupling a portion of the high frequencies to ground. The volume control for the audio is accomplished inside U1001 via the serial bus.

Troubleshooting

The best approach in troubleshooting audio is to signal trace the audio with an oscilloscope. Once the circuit area causing the problem is located, voltage and resistance checks can localize the defective components.
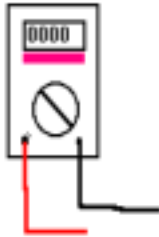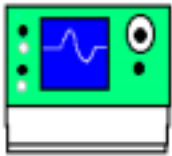
No Audio

1. Check pin 3 on U1001 for wideband audio out. This is a good midpoint in the circuit to start. If no audio is present, the problem may be related to the IF circuit. Confirm by connecting an audio source to the Aux input jacks (on sets that have them). If audio is present at pin 3, go to the next step.

2. Check for audio out of pins 13 and 14 of U1701, the stereo decoder. If no audio is present, suspect U1701, the supply to pin 19 or a defective coupling capacitor in the decoder circuit. If the audio is present, go to the next step.

3. Check for audio on pins 59 and 60 of U1001. If audio is not present, but is present at U1001 pins 4 and 5, suspect U1001. If it is present, go to the next step.

4. Check for audio in and out of U1901 on pins 5 and 1 for the input, and 8 and 10 for the output. If audio is coming out of the IC, check the signal path out to the speakers. If audio is going in to the IC but not coming out, go to the next step.

5. Check the 26 volts to U1901 at pin 9 and the mute voltage on pin 3. Approximately 12 volts should be on pin 3 when the speakers are not muted.

The PIP (Picture In Picture) circuit superimposes a small picture on to the big picture. **PIP**
Different versions of this circuit are designated by a letter preceding the PIP prefix.
The D-PIP circuit used in the CTC177 has the same functionality as the D-PIP used
in the CTC169; however, there are two primary differences. The D-PIP in the CTC177
is built on to the main chassis circuit board and consists of only two IC's. Because of
the additional integration, the circuit is much simpler and easier to troubleshoot.

TV Video and Aux Video from U1001 are buffered by Q2705 and Q2704 and
capacitively coupled to pins 4 and 8 respectively on U2901, the PIP processor. A
sandcastle signal, comprised of horizontal and vertical blanking along with a burst key
pulse, is input to pin 19 for synchronization purposes. U2901 is controlled via the IM
Bus clock, data and enable lines. Power for the chip is provided by U2903, the 5.4 volt
regulator.

When PIP is activated, internal switches select big and small pix information from pins
8 and 4 of U2901. Either source can be used for big or small pix. Only the composite
video is applied to U2901. There is no provision for S-Video source inputs into PIP.
If an S-VHS VCR is used, the composite video jacks must also be connected.
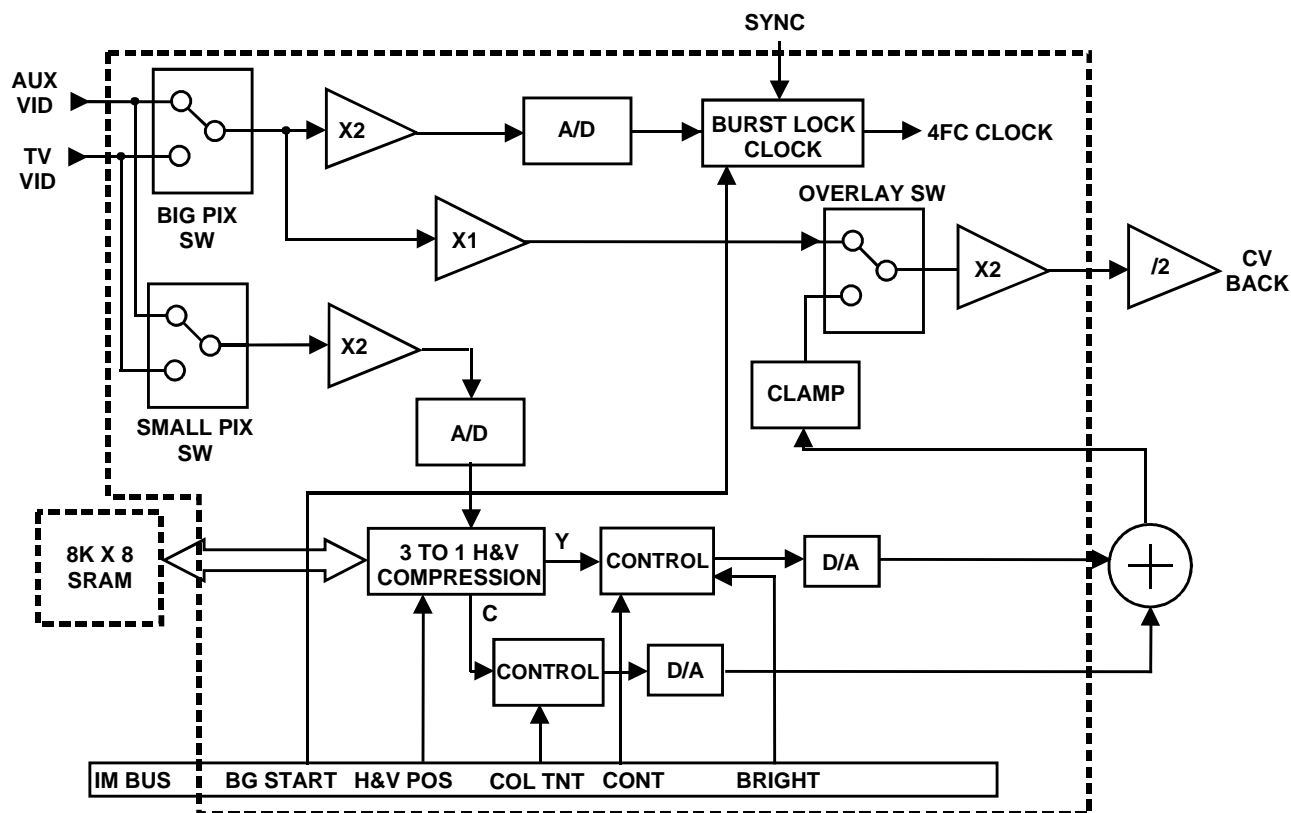
Figure 41, PIP Block Diagram
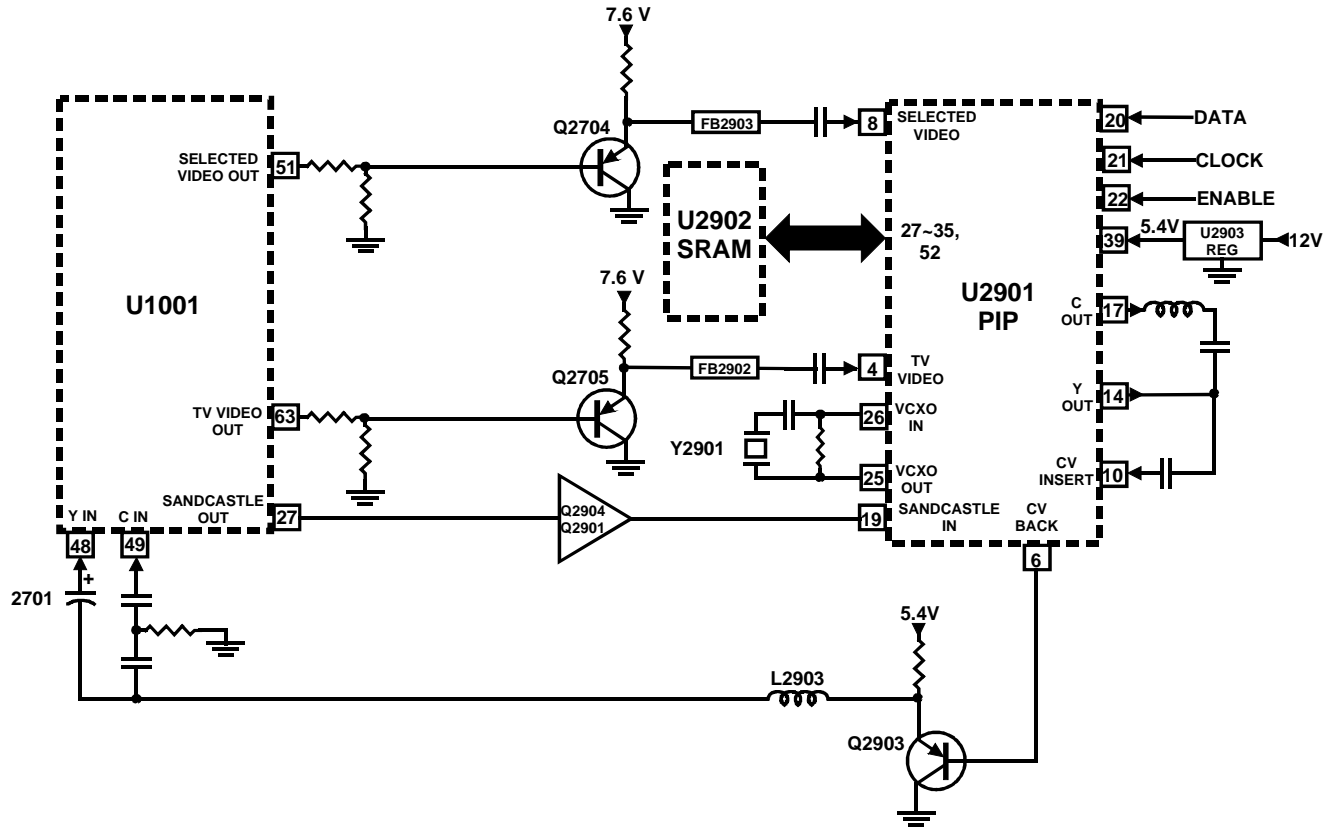
Figure 42, Pip Circuit

Small pix information is compressed 3:1. For every 3 lines of video sampled, 1 is used and 2 are discarded. U2902 is an external SRAM is used for line storage in this process. The timing of the small pix digital circuitry is locked to the big pix burst signal. It is important to remember irregular burst on the big pix source will adversely affect the small pix. Certain video tape copy guard schemes also may cause the PIP circuit not to function correctly.

After processing, the chroma and luma components of the small pix are converted to analog video and exit U2901 at pins 17 and 14. They are summed together to form composite video and re-enter U2901 at pin 10. The signal is then sent to a clamp circuit. It is then applied to the overlay switch where it is inserted into the big pix signal. The overlay switch is internal to U2901 unlike the CTC169 version. Composite video containing the big and small pix information is output from pin 6 and is sent back to U1001. The luma and chroma are separated by filtering and input separately to pins 48 and 49 of U1001.

There are four user controls:

- Move
- Swap
- Freeze
- PIP on/off

Move allows the customer to move the small picture to any of the four quadrants on the screen. Swap enables the user to trade the small pix for the big pix and vice versa. Freeze will digitally store the small pix and display a still frame picture for the small pix. PIP on/off turns the PIP feature on or off.

PIP like the other circuits on the chassis is controlled over the serial bus. There are no analog alignments of this PIP circuit as in the CTC169. The following alignment parameters are set via the service menu with the remote control:

- Chroma Gain
- Tint
- Brightness
- Contrast

1. Enter parameter #23 for chroma level adjustment. Adjust value level to match big pix chroma level. Do not set the adjustment very far away from the initial factory setting.

2. Enter parameter #24 for tint phase adjustment. Adjust value to match the big pix tint phase. Do not set the adjustment very far away from the initial factory setting.

3. Enter parameter #25 for brightness level adjustment. Adjust the value level to match the big pix brightness level. The smaller the number, the brighter the picture.

4. Enter parameter #26 for contrast level adjustment. Adjust value level to match big pix contrast level.

The increased level of integration makes troubleshooting the PIP circuit very easy and straight forward. Signal tracing the video signal through the circuit with an oscilloscope is the best approach. Bypassing the PIP circuit is possible by unsoldering L2903 and connecting the emitter of Q2704 to the negative side of the capacitor connected to U1001 pin 48 (C2701); however, because of the fragile nature of the copper traces on the Glasteel circuit board, soldering should only be done when absolutely necessary. Signal tracing with the oscilloscope is the preferred method.
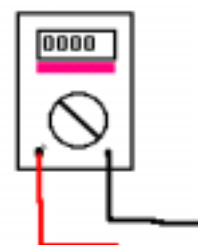
No Big or Small Pix

All video is routed through the PIP circuit. A complete failure of the PIP circuit will cause a no video symptom. The audio and OSD are unaffected by a PIP malfunction. If there is no audio and/or OSD, the PIP circuit is not the problem.

1. Push the PIP button on the remote control and see if the OSD indicates the PIP function. If this does not happen, the TV may have the wrong or defective U3201, EEPROM. The EEPROM determines the features of the set. An EEPROM from the same chassis without PIP will not let the micro address U2901. If U2901 is not initialized by the microprocessor (the EEPROM tells the micro U2901 is there), the internal video switches can land in any random position. If the switches do not land in the bypass position, video will not pass through the circuit.

2. Check the Aux and TV video sources on FB2903 and FB2902. If the video is not present, trace back towards U1001 pins 51 and 63. If the video is present on the ferrite bead jumpers, go to the next step.

3. Check for composite video at pin 6 of U2901. If the signal is not there, troubleshoot U2901: the clock, data and enable lines; the supply to pin 39; and the oscillator at pins 25 and 26. If video is present at pin 6, go to the next step.

4. Check for video on L2903. If it is not present, suspect a defective Q2903. If it is there check the signal path to pins 48 and 49 of U1001.

No Small Pix

It is possible for a PIP malfunction to allow the big pix information to pass through but not the small pix. U2901 is controlled over the serial bus by U3101. As stated above, the internal switching of U2901 can let video pass though while U2901 is inoperative.

1. Verify the OSD indicates PIP. If it does not, there is a system control problem, not a PIP problem.

2. Check for horizontal and vertical sync at pin 19 of U2901. If the sync is not present, the small pix will not turn on.

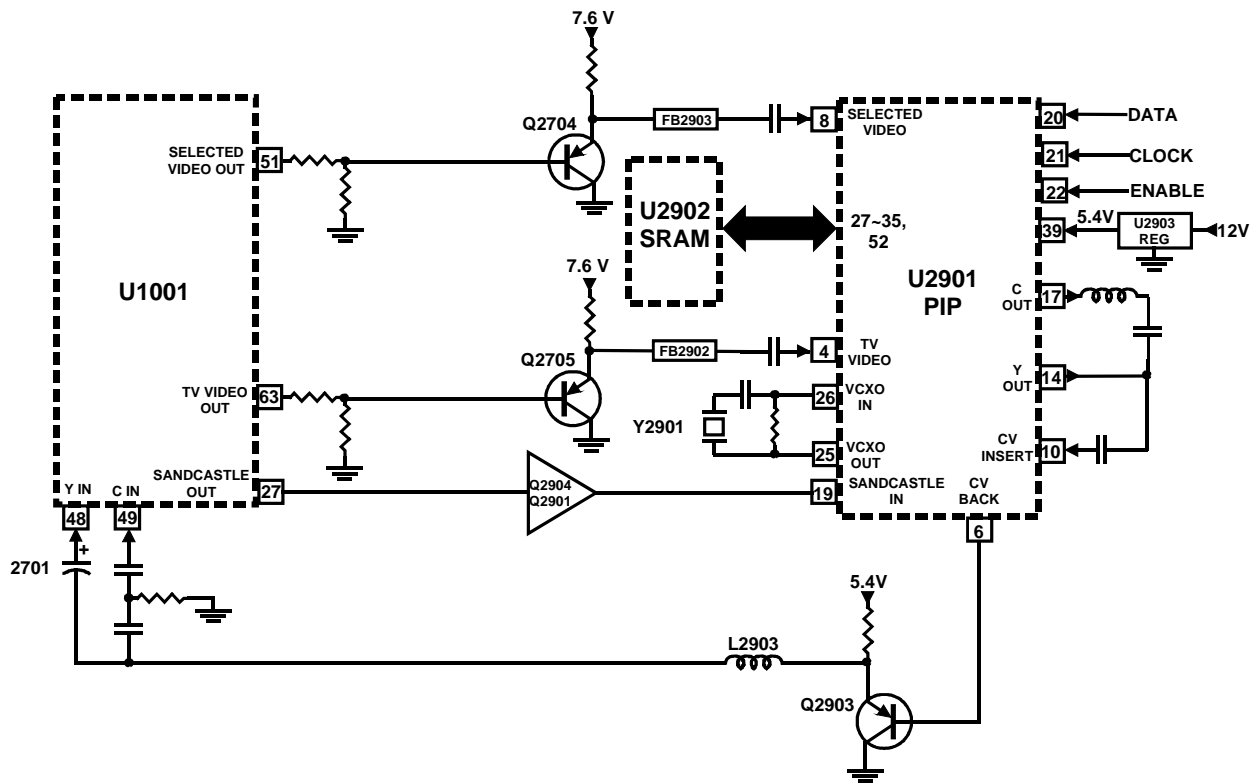3. Check the oscillator at pins 25 and 26. If the oscillator is not present, the small pix will not turn on.

Figure 43, PIP Circuit (repeated)

PIP - Top View

Figure 44, PIP (Top View)

PIP Circuit - Bottom View

Figure 45, PIP Circuit (Bottom View)

U3101   System   Control   Microprocessor

PIN NO.	NAME	VOLTAGE	IN CKT. RES.	DESCRIPTION
1	RESET	5.0	>200K	Micro reset - Active LO
2	DATA IN	4.8	>200K	Data input for commercial television.
3	IR IN	4.5	>300K	IR input signal from remote control.
4	DEGAUSS	0	>20M	Activate degaussing relay.
5	KD1	0	>20M	Keyboard drive line.
6	KS1	4.7	>200K	Keyboard scan input.
7	KS2	4.7	>200K	Keyboard scan input.
8	KS3	4.7	>200K	Keyboard scan input.
9	DATA OUT	.3	>20M	Data out for commercial television.
10	NC	-	-	-
11	ATE ENABLE	0	10K	Used for factory testing.
12	PIP ENABLE	4.7	>20M	Serial com. line used to control data between the micro and PIP.
13	CC VIDEO	* VARIES WITH MODEL	VARIES WITH MODEL	Closed caption video input.
14	T-CHIP ENBL	4.6	>20M	Serial com line used to control data between the micro and T-Chip.
15	T-CHIP DATA TUNER CLK	4.5	>20M	Serial communication data/clock line.
16	T-CHIP CLK TUNER DATA	4.7	>200K	Serial communication data/clock line.
17	BLUE OSD	O	VARIES WITH MODEL	Blue OSD output.
18	GREEN OSD	O	1K	Green OSD output.
19	RED OSD	O	VARIES WITH MODEL	Red OSD output.
20	VDD	4.7	>20M	+5 VDC.
21	VSS	0	0	Ground.
22	FAST SWITCH	0	2K	Fast Switch - controls OSD and video switching in T-Chip.
23	STEREO/MONO/NWS	* VARIES	70K	Selects Stereo, Mono or National Weather Service.
24	H	.7	8K	Horizontal timing input for OSD.
25	V	.2	1.8K	Vertical timing input for OSD.
26	R1	2.0	10K	OSD PLL external control pin.
27	VCO	2.0	>20M	OSD VCO external control pin.
28	NC	-	-	-
29	SPKR MUTE	0	>100K	Goes HI to mute speakers.
30	TONE	0/5	>100K	Goes HI for low tone and LO for high tone.
31	FM ON/OFF	0	>20M	Turns the FM receiver On/Off - Commercial television only.
32	STEREO SENSE	0/5	63K	Input used to detect the presense of a stereo broadcast.
33	FM TUNED	* VARIES	>20M	Input to detect when an FM station is tuned - Commercial television only.
34	RF SEC	* VARIES	>20M	PWM output - controls secondary of double tuned filter in the tuner.
35	RF PRI	* VARIES	>20M	PWM output - controls primary of double tuned filter in the tuner.
36	SINGLE TUNE	* VARIES	>20M	PWM output - controls single tuned filter in the tuner.
37	STBY SW	-	-	-
38	NC	-	-	-
39	TUNING SYNC	2.3	>20M	Sync input to detect the presense of an active channel when tuning.
40	IF DEFEAT	0	>20M	Output that can be used to defeat the IF circuit via AGC.
41	OSC 2	2.3	4M	4 MHz Oscillator.
42	OSC 1	2.3	3.5M	4 MHZ Oscillator.

U1001 (T-CHIP)

PIN NO.	SIGNAL NAME	APPROX. VOLTAGE	IN CKT. RES. (-GND)	DESCRIPTION
1	Aux Video In	1.5	>20M	Input for external composite video.
2	IF Vcc	7.6	500	Power source for IF circuits inside T-Chip.
3	WB Audio Out	3.8	>20M	Detected Wideband audio out of the T-Chip
4	TV Left In	5.0	>20M	Left channel audio input.from stereo decoder.
5	TV Right In	5.0	>20M	Right channel audio input. from stereo decoder.
6	PIF APC Filter	3.7	>20M	External filter connection for IF VCO.
7	Aux Left In	5.0	>20M	Left channel audio input from external jacks.
8	Aux Right In	5.0	>20M	Right channel audio inputs from external audio jacks.
9	IF Ground	0	0	Ground connection for IF circuits.
10	IF 1 In	3.6	22K	IF input from tuner.
11	IF 2 In	3.6	22K	IF input from tuner.
12	RF AGC Out	4.5	50K	RF AGC control output to the tuner.
13	AGC 1	4.8	>20M	External connection to the AGC circuit for gain control.
14	AGC 2	4.8	>20M	External connection to the AGC circuit for gain control.
15	3.58 Crystal	3.1	>20M	3.58 MHz crystal point.
16	Size Comp.	1.5	1.5K	Allows vertical height to track beam current to prevent blooming.
17	Vert. Output	8.3	8.3K	Vertical ramp drive output.
18	Vert. ALC	3.2	>20M	Filter connection to Automatic Level Control for vertical drive.
19	E-W Out	3.0	>100K	Vertical parabola for E-W pincushion correction.
20	Ref I	1.0	1.6K	Internal horizontal reference current path.
21	Horz. GND	0	0	Ground path for internal horizontal circuitry.
22	Standby Vcc.	7.6	6.7K	Input for the 7.6 volt standby voltage to start horizontal.
23	APC Filter	2.6	>20M	Filter connection for horizontal APC.
24	Horz. Out	3.0	12K	Horizontal drive output.
25	Flyback In	1.3	24K	Feedback input from flyback for phase correction.
26	XRP	.05	32K	Xray protection shutdown pin.
27	Sandcastle Out	1.2	21K	Sandcastle signal output. Contains H&V blanking with burst gate.
28	PWM Out	0	1K	Not Utilized.
29	PWM Comp	3.6	>20M	Error amplifier output to control linear B+ reg. on CTC175 only.
30	PWM In	3.7	>20M	Error amp feedback input from CTC175 power supply.
31	Beam Sense	7.0	2K	Input for beam limit. Beam limit active below 6.2 volts.
32	Vid/Vert Vcc	7.6	500	Vcc input for the video and vertical circuits in the T-Chip.

U1001 (T-CHIP)

PIN NO.	SIGNAL NAME	APPROX. VOLTAGE	IN CKT. RES. (-GND)	DESCRIPTION
33	Vid/Vert GND	0	0	Ground path for the video and vertical circuits inside the T-Chip.
34	Pix ABL Filter	2.7	>100K	External filter connection for Pix ABL circuit.
35	Brt ABL Filter	2.8	>20M	External filter connection for BRT ABL circuit.
36	Red Out	3.0	>20M	Red output to CRT.
37	Green Out	2.7	>20M	Green output to CRT.
38	Blue Out	3.0	>20M	Blue Output to CRT.
39	Fast Switch In	0	1.5K	Fast switch input from micro to control OSD/Video switching.
40	Red In	0, *VARIES	>20M	Red OSD input from micro.
41	Green In	5.5	>20M	Green OSD input from micro.
42	Blue In	5.5	>20M	Blue OSD input from micro.
43	Black Lev Det	4.7	>300K	External filter connection for the Black Stretch Circuit.
44	Select Y Out	4.0	>20M	Selected Y out signal used as Closed Caption video source.
45	Y2 In	3.8	>20M	S-Video luminance input.
46	C2 In	3.1	>20M	S-Video chroma input.
47	Color Killer	3.8	8K	Color killer filter connection.
48	Y1 In	3.9	>20M	TV luminance input.
49	C1 In	3.1	>20M	TV chroma input.
50	Filt Tst It	5.5	>20M	Autotune filter connection. Used to lock all internal oscillators.
51	Select Vid Out	3.2	2K	Selected video (Aux/IF) out to PIP.
52	Bus Enable	4.6	>20M	T-Bus enable from micro. Used to control data to and from T-Chip.
53	Bus Clock	4.7	>1M	T-Bus clock used to synchronize data transfers.
54	Bus Data	4.6	>20M	T-Bus data from micro.
55	Snd IF Out	3.7	>20M	Sound IF out of T-Chip. Sent to 4.5 MHz CF and input to pin 58.
56	Bus Ground	0	0	Ground connection for T-Bus.
57	Audio Bias	5.8	>20M	External filter connection for audio bias circuitry inside T-Chip.
58	Snd IF In	2.55	8K	Input for 4.5 MHz filtered sound IF.
59	Right Out	3.8	>20M	Right channel audio output from T-Chip.
60	Left Out	3.8	>20M	Left channel audio output from T-Chip.
61	Vol DAC Fltr	.96	>20M	Filter connection for audio volume DAC.
62	VCO Tank 2	6.6	1.5K	External connection to video VCO tank circuit.
63	Video Out	3.2	2K	Detected video output.
64	VCO Tank 1	6.6	1.5K	External connection to video VCO tank circuit.

U1001 (T-CHIP) Internal Block Diagram

U1001

IF VCO

VCC

SND IF

4.5 TRAP

VID AMP

NIV

IF AMP

RF AGC

IF AGC

BUS DECODER

CHROMA VCO

AUTOFLESH

2nd AMP

CHROMA FILTER

1st AMP

VERT SIZE

BLACK STRETCH

LUMA FILTER

PARABOLA GENERATOR

VERT RAMP GENERATOR

SYNC SEP

REG

VERT C/D

PIX

INT/EXT SWITCH

R-Y

B-Y

Y

EXT RGB MATRIX

1ST AFC

HOR VCO

HOR C/D

2ND AFC

HOR OUT

BRIGHTNESS

MATRIX

Σ DRIVE BIAS BLANK

Σ DRIVE BIAS BLANK

Σ DRIVE BIAS BLANK

SWITCHING REGULATOR

BEAM LIMITER

VCC

Pin numbers: 1–32 (left side), 33–64 (right side)

Index

CTC 176/177 BLOCK DIAGRAM

CTC175/176/177 Self-Test

Select the best answer(s) to the questions.
Exercise #1

1. Why would the differences between a "hot chassis" and a "cold chassis" have an effect on what features could be supported by the chassis, for example, PIP, video jacks, etc.?
   A. The "Hot Chassis" runs warmer than the "Cold Chassis."
   B. A "Hot Chassis" poses a safety hazard with exposed metal parts. Hence, external jacks are prohibited.
   C. There are no differences.
   D. The "Hot Chassis" can support more features.

2. Why is it necessary to hook up the composite video jacks even if an S-Video source is being used?
   A. S-Video is not routed through the PIP circuit so composite video is needed for the small pix source.
   B. It is not necessary. It merely ensures at least one of them will be hooked up correctly.
   C. The S-Video source is not the correct level for the PIP circuit.
   D. None of the above.

3. What function does R4104 in the CTC176/177 power supply serve?
   A. It is a bleeder resistor.
   B. It minimizes voltage spikes.
   C. It is the start-up resistor for the power supply.
   D. All of the above.

4. What symptom would you expect if R4104 were open?
   A. It would be hard to tell.
   B. Dead Set.
   C. Pulsing set.
   D. Audible squeal.

5. What function do C4123 and R4125 serve?
   A. High voltage spike filtering.
   B. Standby error amplifier.
   C. Oscillating feedback path.
   D. None of the above.

6. R4124 is the source resistor for the switching FET inside U4101. What happens to the voltage drop across R4124 as the load on the power supply increases?
   A. Increases.
   B. Decreases.
   C. Stays the same.
   D. None of the above.

7. What will happen to the CTC177/176 power supply if the load increases beyond what is considered normal operating parameters?
   A. The TV will self-destruct.
   B. Shutdown.
   C. Display "Overload" on the screen.
   D. None of the above.

8. What is the normal operating voltage for the error amp on pin 1 of U4101?
   A. 100 volts.
   B. -100 volts.
   C. -20 volts.
   D. None of the above.

9. If the switching power supply frequency is in the audible range, what is the cause?
   A. Mis-adjusted frequency.
   B. Line voltage is too high.
   C. An excessive load on the power supply.
   D. None of the above.

Exercise #2

1. What IC's actively make up the system control circuit?
   A. U3101 & U3201.
   B. U2901 & U7401.
   C. U1001.
   D. All of the above.

2. Where are all the digital alignments for the chassis stored?
   A. U3201.
   B. U1001.
   C. U7401.
   D. U2901.

3. What is the purpose of the reset circuit and what does the television do when the reset circuit is active?
   A. Starts the micro in a known place in its program. The television off when reset is active.
   B. Starts the micro in a known place in its program. The television is on when reset is active.
   C. Prevents the TV from being turned on too soon.
   D. None of the above.

4. How does U3101 turn on the television?
   A. Pulls the on/off pin on the micro HI.
   B. Pulls the on/off pin on the micro LO.
   C. Sends an on command to the T-Chip over the serial bus.
   D. None of the above.

5. What kind of data activity is present on the serial bus in the standby mode on a normally functioning set?
   A. No data activity is noticeably present.
   B. Data activity is seen constantly.
   C. 5 Vpp pulses.
   D. None of the above.

6. What will be seen on the serial bus if U3201 is missing or defective?
   A. Nothing.
   B. Constant data activity as U3101 looks for U3201.
   C. Partial data activity.
   D. None of the above.

7. How does U3101 know when the television is in XRP shutdown?
   A. It doesn't know. There is no XRP pin to the micro.
   B. By monitoring the scan supplies.
   C. By looking at the XRP bit in the T-Bus data sent from U1001.
   D. None of the above.

8. How does U3101 detect the presence of S-Video?
   A. Checks the horizontal lock bit in the T-Bus data.
   B. It gets information from the S-Video detector IC.
   C. By the user selecting S-Video.
   D. None of the above.

9. What information is stored in the U3201, the EEPROM?
   A. Channel scan list and labels.
   B. All digital alignments.
   C. The TV serial number.
   D. None of the above.

10. What will the technician have to do if the EEPROM is replaced?
   A. The EEPROM comes pre-aligned and will require the technician to do nothing.
   B. Re-align the entire chassis.
   C. Re-align only the tuner.
   D. None of the above.

11. Where in the video signal is the closed caption signal sent?
   A. In the audio carrier.
   B. On line 19 of the video signal.
   C. On line 21 of the first field of video.
   D. None of the above.

12. What is the password to get to the first level of alignments?
    A. 9,900,000.
    B. 95.
    C. 125.
    D. None of the above.

13. How does U3101 know if the *Power* button or the *Channel* button has been pressed?
    A. By using two drive lines.
    B. By monitoring the keyboard sense lines for a constant or pulsing LO.
    C. By a looking for a HI at the *Power* and *Channel* pins on the micro.
    D. None of the above.

Exercise #3

1. What is the difference between the 20" and 25" horizontal deflection circuit verses the 27" and 31" horizontal deflection circuit?
    A. Pincushion circuit.
    B. Horizontal output circuit.
    C. No differences. Everything is compensated for in the yoke.
    D. None of the above.

2. Are the horizontal output transistors, Q4401, the same part for the 25" and 27"?
    A. Yes.
    B. No.
    C. Depends on the model.
    D. None of the above.

3. Symptom: The picture is shifted to the right, but is locked. What horizontal circuit (or alignment) is most likely at fault?
    A. Horizontal APC.
    B. Horizontal AFC.
    C. Horizontal linearity.
    D. None of the above.

4. Symptom: The picture is tearing diagonally and the horizontal circuit is making a squealing sound. What horizontal circuit (or alignment) is most likely at fault?
    A. Horizontal APC.
    B. Horizontal AFC.
    C. Horizontal linearity.
    D. None of the above.

5. If the horizontal frequency alignment is set too low, what will happen?
   A. The TV will operate normally but will make a squealing sound.
   B. The TV will shutdown.
   C. The picture will collapse vertically.
   D. None of the above.

6. How can the technician overcome the problem induced in the previous question?
   A. Replace the EEPROM.
   B. Temporarily install additional capacitance in the horizontal output circuit to bring high voltage down far enough to start the set.
   C. The problem cannot be overcome.
   D. None of the above.

7. What screen sizes have a pincushion correction circuit?
   A. 20".
   B. 25".
   C. 27".
   D. 31".

8. A repeat failure of the vertical output IC, U4501, can be caused by what?
   A. Pincushion circuit.
   B. IF circuit.
   C. System control circuit.
   D. None of the above.

9. What is the 7.6 volt supply to pin 22 of U1001 used for?
   A. Keeps the data bus in U1001 active.
   B. Provides the necessary bias to the horizontal drive circuits in order to start the TV.
   C. Keeps the TV in the off mode.
   D. All of the above.

10. One terminal of the vertical yoke connector (E4501) is tied to the "half supply" derived off the 12 volt run supply. What voltage on E4502 will cause the electron beam to be at approximately the center of the screen?
   A. 0 volts.
   B. 5 volts.
   C. Approximately 12 volts.
   D. Approximately 26 volts.

11. What is the average DC level of the vertical ramp at pin 17 of U1001?
    A. 3.8 volts.
    B. 7.6 volts.
    C. 12 volts.
    D. 26 volts.

12. What is the purpose of the vertical size compensation at pin 16 of U1001?
    A. Increases vertical height during high beam current scenes.
    B. Decreases vertical height during high beam current scenes.
    C. It is part of the error amplifier for linear regulator.
    D. All of the above.

Exercise #4

1. What is the advantage (as far as tuning channels) of the CTC177 tuner over the traditional "track" tuner?
    A. There is no advantage.
    B. The tuner can more accurately tune channels individually by independently adjusting the stages of the tuner.
    C. Can tuner many more channels than previous tuners.
    D. None of the above.

2. Where are the alignment data for the tuner stored?
    A. U3101.
    B. U3201.
    C. U1001.
    D. None of the above.

3. How many alignments are there for each of the alignment channels?
    A. 1.
    B. 2.
    C. 3.
    D. 4

4. How many alignment channels are there and why?
    A. 19.
    B. 125.
    C. Cover the entire frequency range of the tuner.
    D. Conserves memory in the EEPROM and allows linear interpolation to tune in-between channels.

5. If one alignment channel is re-aligned, why should they all should be re-aligned?
    A. Changing one channel will alter the linear interpolation curve possibly causing channels to be mis-tuned.
    B. All alignments are erased when one channel alignment is changed.
    C. All channel alignments must be stored at the same time.
    D. None of the above.

6. Why if one varactor diode in either the UHF or VHF circuit is changed, all of the varactor diodes in the respective circuit must be changed.
   A. It is cheaper to replace them all instead of just one.
   B. The diodes are matched for junction capacitance. If only one is changed, the tuner may not operate correctly.
   C. They are located on the board such that unsoldering one will remove the solder to the rest of them.
   D. None of the above.

7. If the tuner will tune all the bands but one, what IC's can be considered to be working properly?
   A. U7501 & U3101.
   B. U3201
   C. At least part of U7401 & U7301.
   D. All of the above.

8. What is the purpose of the isolation box found on the CTC175 tuner?
   A. Minimize RF interference.
   B. Increase the gain of the tuner.
   C. Isolate the antenna connector from the chassis ground.
   D. None of the above.

9. Why is it important the tuner alignment channels be aligned on accurate FCC frequencies?
   A. Maintain compatibility with different cable systems.
   B. It is an FCC requirement.
   C. Decreases the alignment steps.
   D. None of the above.

10. What are the steps for aligning the data channels on the tuner with the service menu?
   A. Monitor the AGC voltage.
   B. Adjust the secondary, primary and single tuned filters.
   C. Adjust for lowest AGC voltage.
   D. All of the above.

Exercise #5

1. How is AFT carried out in the CTC177 chassis?
   A. AFT voltage is sent back to U3101.
   B. The wide band amplifier controls the PLL.
   C. Digital frequency inside U1001 sends AFT information over the serial bus to U3101.
   D. None of the above.

2. Why is there no AFT alignment necessary on the CTC177 chassis?
    A. The AFT coil is aligned at the factory and requires no further adjustment.
    B. There is no AFT coil because digital AFT uses a frequency counter.
    C. The AFT adjustment is auto programmed.
    D. None of the above.

3. What are the three possible luminance sources on a fully featured CTC177 ?
    A. IF video .
    B. Aux Video.
    C. S-Video.
    D. None of the above.

 4. How is OSD mixed with the rest of the video?
    A. OSD lines are wired to the CRT socket board where the individual guns are biased.
    B. Inside the RGB IC.
    C. OSD information from U3101 is sent to U1001 where it is mixed internally with the video.
    D. None or the above.

5. If pin 39 were a constant HI, even with no OSD present, what would be the symptom on the screen?
    A. Red video.
    B. Green video.
    C. No video.
    D. None of the above

6. Why can't the 3.58 MHz chroma oscillator be monitored outside U1001?
    A. The oscilloscope will load down the oscillator.
    B. The crystal is connected in series with a comparator and is a null point.
    C. There is no 3.58MHz crystal.
    D. None of the above.

7. How can the color killer be defeated?
    A. Apply approximately 4 volts in U1001 pin 47.
    B. Ground U1001 pin 47.
    C. Unsolder U1001 pin 47.
    D. Non of the above.

8. Where is the volume control for the audio circuit carried out?
    A. In the audio output IC.
    B. Inside U1001.
    C. In the TVB IC.
    D. None of the above.

9. If the stereo prompt on the OSD is displayed but there is no audio, what portion of the audio circuit can be assumed to be good?
    A. Audio IF circuit.
    B. At least part of the stereo decoder circuit.
    C. The audio output circuit
    D. None of the above.

10. If the voltage on pin 29 of U3101 is LO and the voltage on pin 3 of U1901 is low, what symptom will be exhibited and what component would be a likely suspect?
    A. No audio, U3101.
    B. No audio, Q1903.
    C. Loud audio, U3101.
    D. None of the above.

Exercise #6

1. What are the two big differences between the PIP circuit in the CTC177 and the PIP circuits in the CTC169?
    A. Has more features.
    B. It is built on the main circuit board.
    C. It is primarily composed of only two IC's.
    D. All of the above.

2. If the big picture signal does not contain burst, what symptom would most likely be encountered on the insert picture?
    A. No insert picture at all.
    B. No luminance in the small picture.
    C. No chroma in the small picture.
    D. None of the above.

3. What alignments in the PIP circuit are set over the serial bus using the service menu?
    A. Chroma gain.
    B. Tint.
    C. Brightness.
    D. Contrast.

4. A complete failure of the PIP circuit would most likely create what type of symptom on the screen?
    A. No small pix.
    B. No large pix.
    C. No video at all.
    D. None of the above.

5. When troubleshooting a suspected PIP problem, if the OSD does not indicate PIP, what can be assumed?
   A. The PIP circuit is definitely defective.
   B. System control is the problem.
   C. PIP is not the problem.
   D. None of the above.

6. If the small picture does not work but the OSD does indicate PIP, what two signals should be confirmed?
   A. 3.58 MHz oscillator.
   B. U2901 oscillator.
   C. Sandcastle signal at U2901 pin 19.
   D. None of the above.

7. What are two good test points located on the top of the circuit board to check selected video and TV video going to the PIP circuit?
   A. TP 2606.
   B. FB 2903.
   C. TP 2301.
   D. FB 2902.

8. If PIP operates normally but malfunctions when only certain video tapes are used, what could be the problem?
   A. Bad VCR.
   B. Bad Tape.
   C. Copy guard interference.
   D. All of the above.

9. What are the four user controls with the PIP circuit?
   A. Move .
   B. Swap.
   C. Freeze.
   D. PIP on/off

10. Does the CTC177 contain a comb filter?
   A. Yes.
   B. No.
   C. Depends on model number.
   D. 27" and higher TV's contain the comb filter.